Conceptual design of plasmon-generated programable logic circuit v2.0

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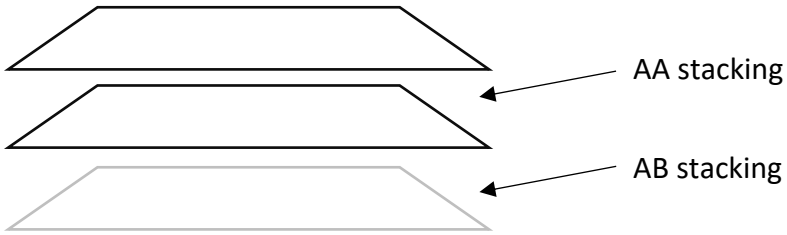
1. Components

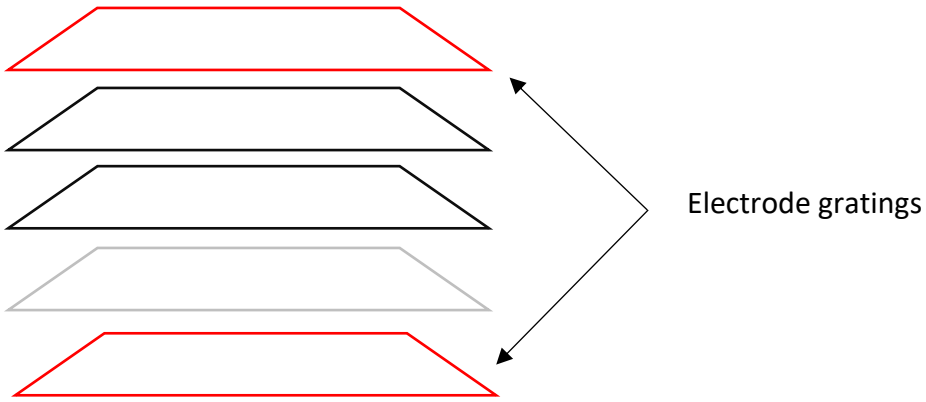
1) Three graphene sheets
2) Two electrode grating sheets
3) Electrode controller
4) THz signal receiver
5) THz signal transmitter

2. Assembly process

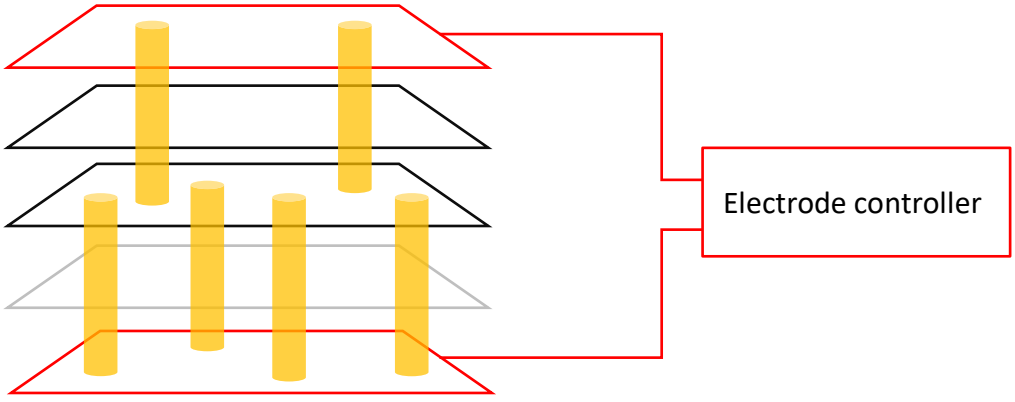
1) Constructing trilaminar graphene with both AA and AB stackings



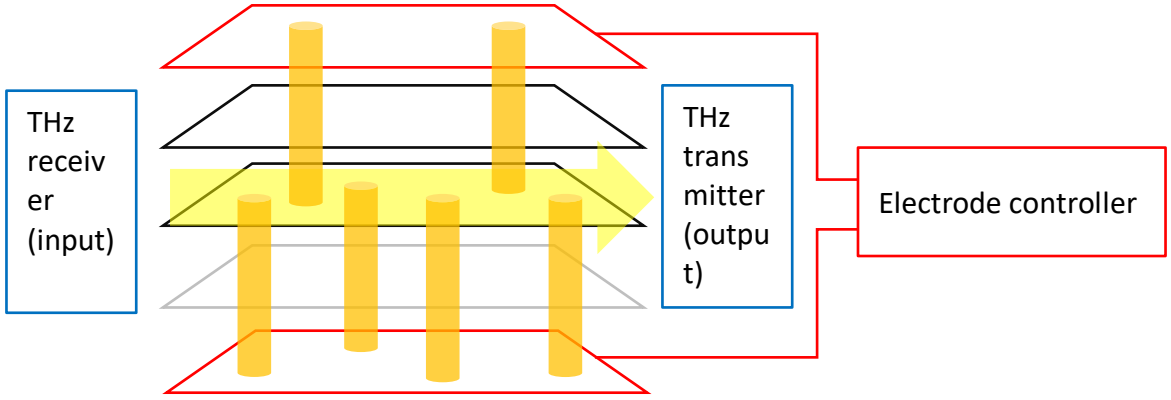
2) Sandwiching graphene sheets between two electrode grating sheets



3) Connecting the electrode controller with the electrodes. This allows us to precisely control the charging patterns on the graphene sheets. This would enable us to generate various logic patterns on trilaminar graphene by adjusting the dot mapping of the electric charges. By combining AA and AB stacking in trilaminar graphene, we would be able to create AND, OR and NOT logics using plasmons generated by the electrode.

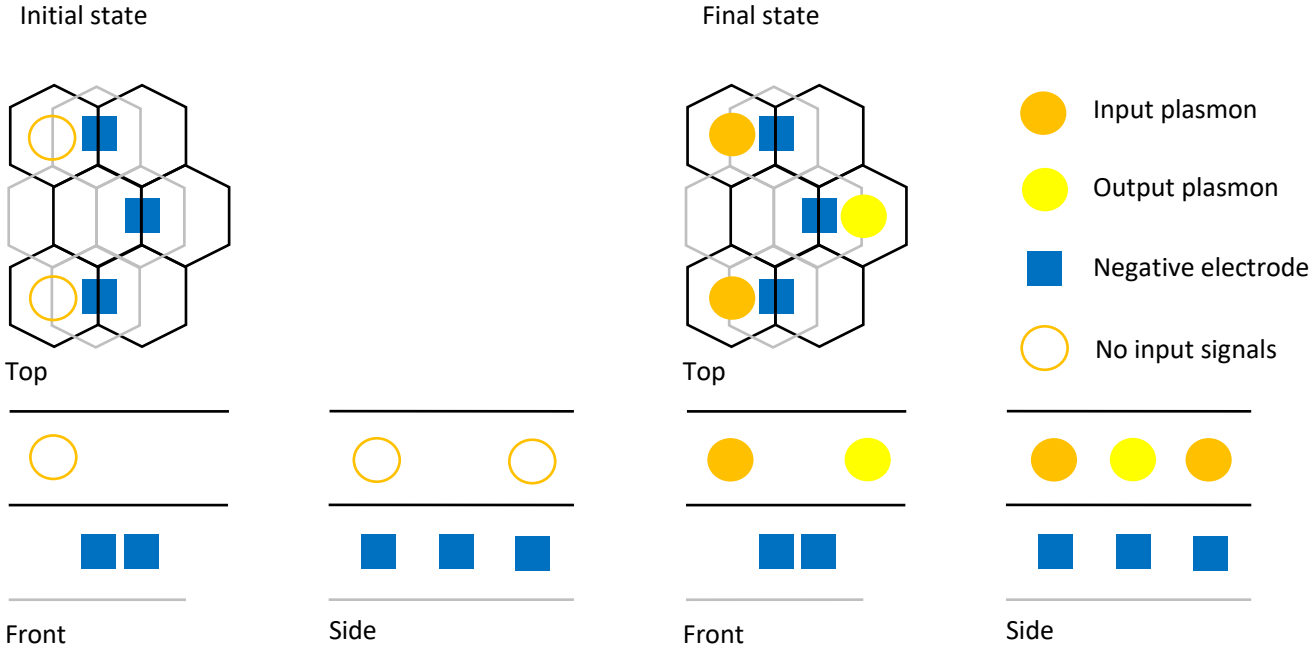


4) Connecting the THz receiver and transmitter to enable transmission of optical digital data, thereby bypassing traditional electrical wire-based data transfer methods. The THz receiver functions as an input module, converting incoming optical signals into plasmons. Meanwhile, the THz transmitter serves as an output module, emitting plasmons in accordance with the processed digital data.

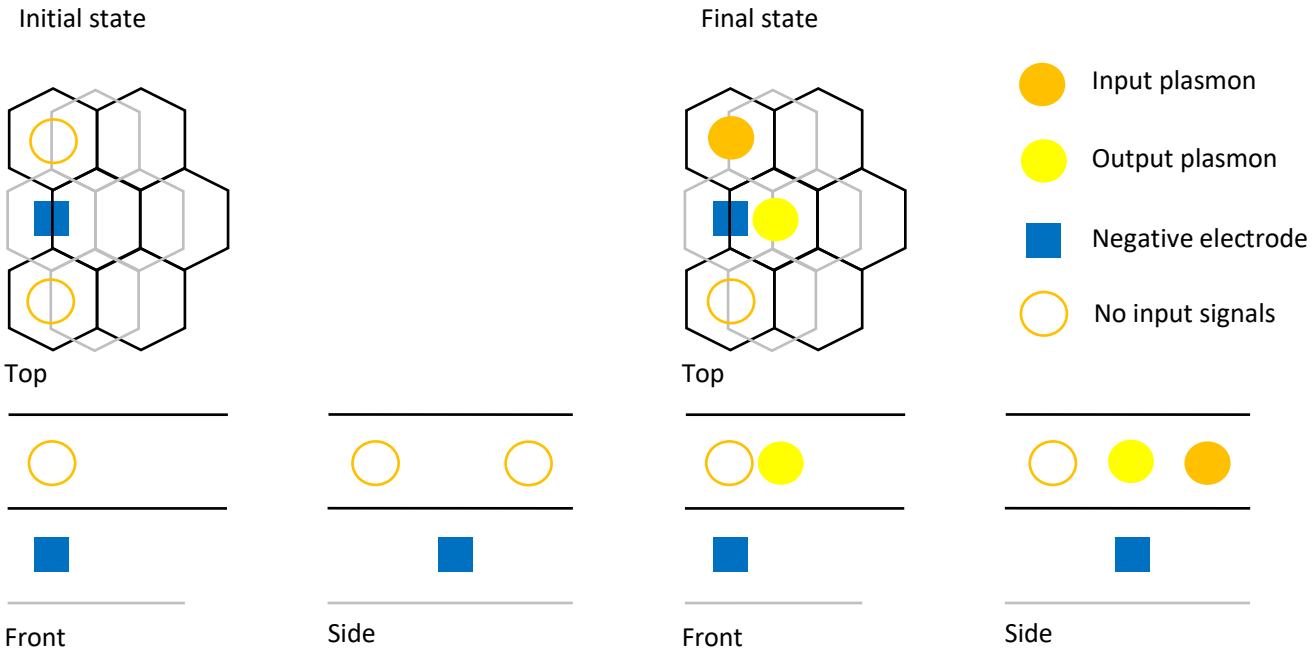


3. Logical procedure

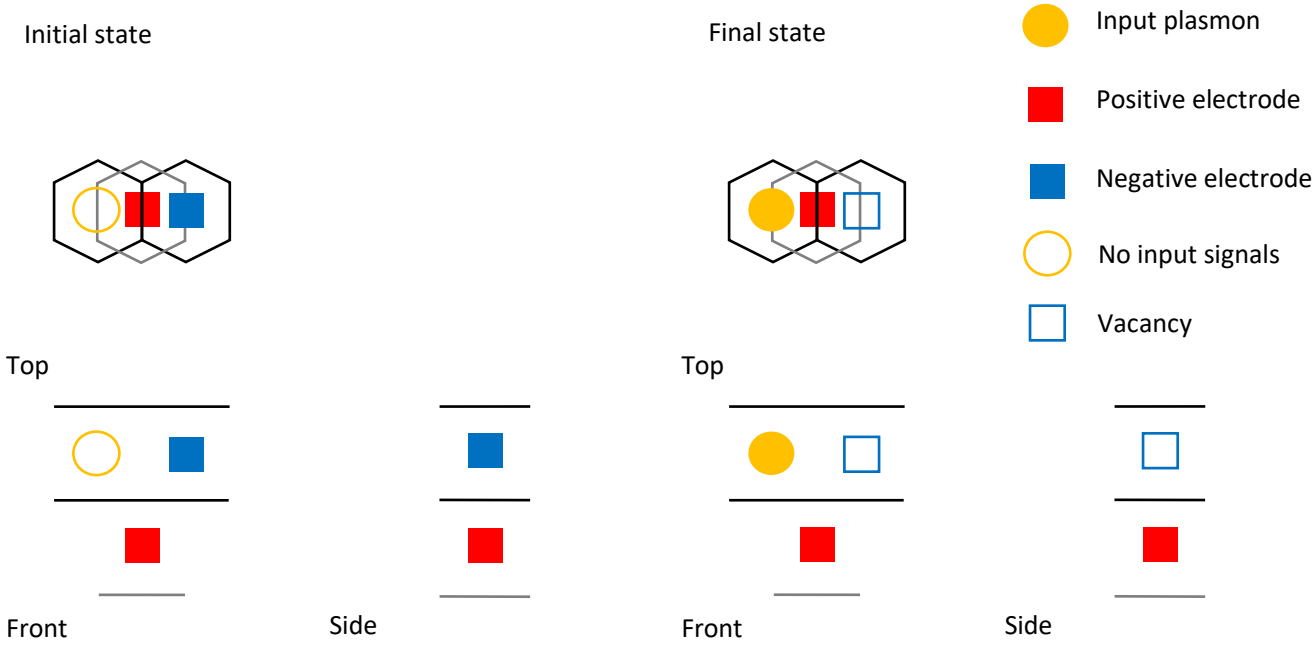
1) AND – The following diagrams show the three views of the AND structure before and after computation. This time we use single honeycomb hole as a bit generator for easier explanation. For the sake of clarity, we have simplified the illustration by focusing on a single honeycomb hole representing the generation of bits. However, in practice, the implementation of the AND gate requires the coordination of multiple honeycomb holes arranged in a specific pattern. When illuminated by a laser beam, the collective plasmons generated by these holes can then be manipulated to perform the desired logic operation. In the AB stacking, three negative electrodes form initially at the interface. In the processing, two input plasmons emerge from the interface in the AA stacking. At the final state, an output plasmon emerge in right side of AA stacking by the overwrapped electric field of two input plasmons. Negative electrodes support the emission of electric fields from the inputs to the output. This procedure is derived from the concept previously written by the author, which can be found at https://github.com/r-coin/basic/blob/master/cqc_edited.pdf.



2) OR – OR logic can be achieved using a negative electrode placed in AB the stacking between two inputs.

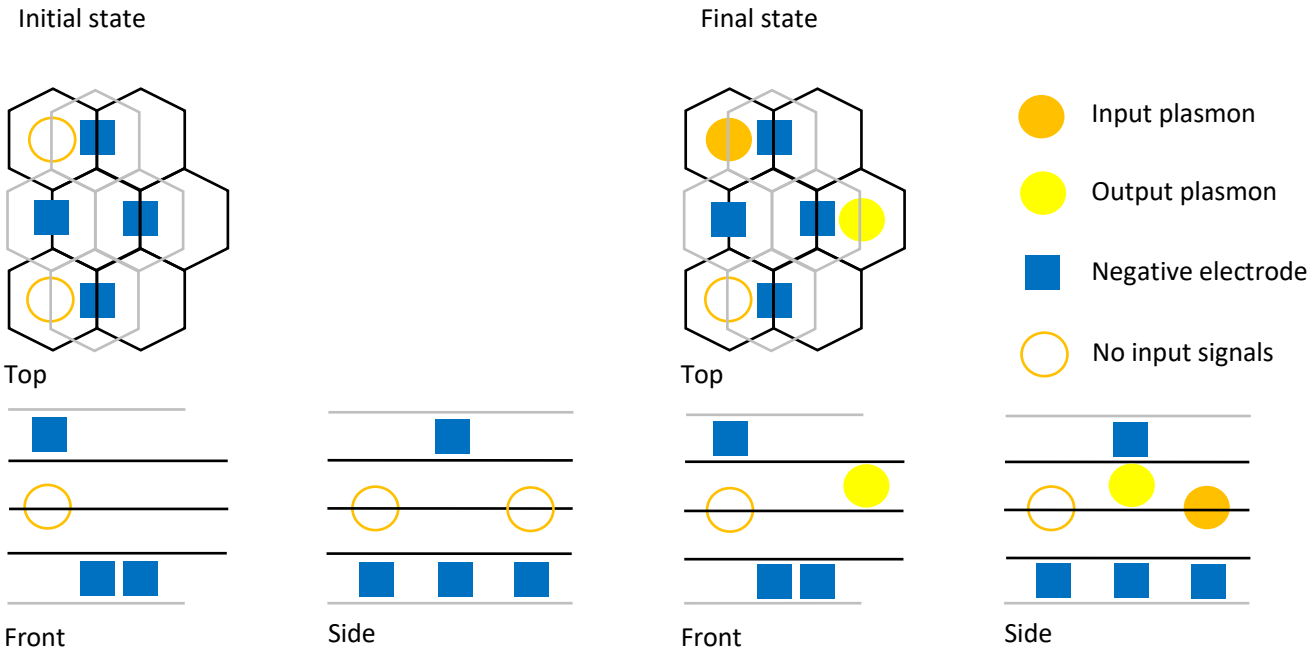


3) NOT – Intuitive ideas for NOT logic are still being explored, but the design includes placing a positive electrode in the AB stacking and a negative electrode in the AA stacking. When the input signal arrives, the negative electrode would drain to positive electrode. For proper functioning of logical operations, we might require adding another graphene layer or implementing certain modifications.

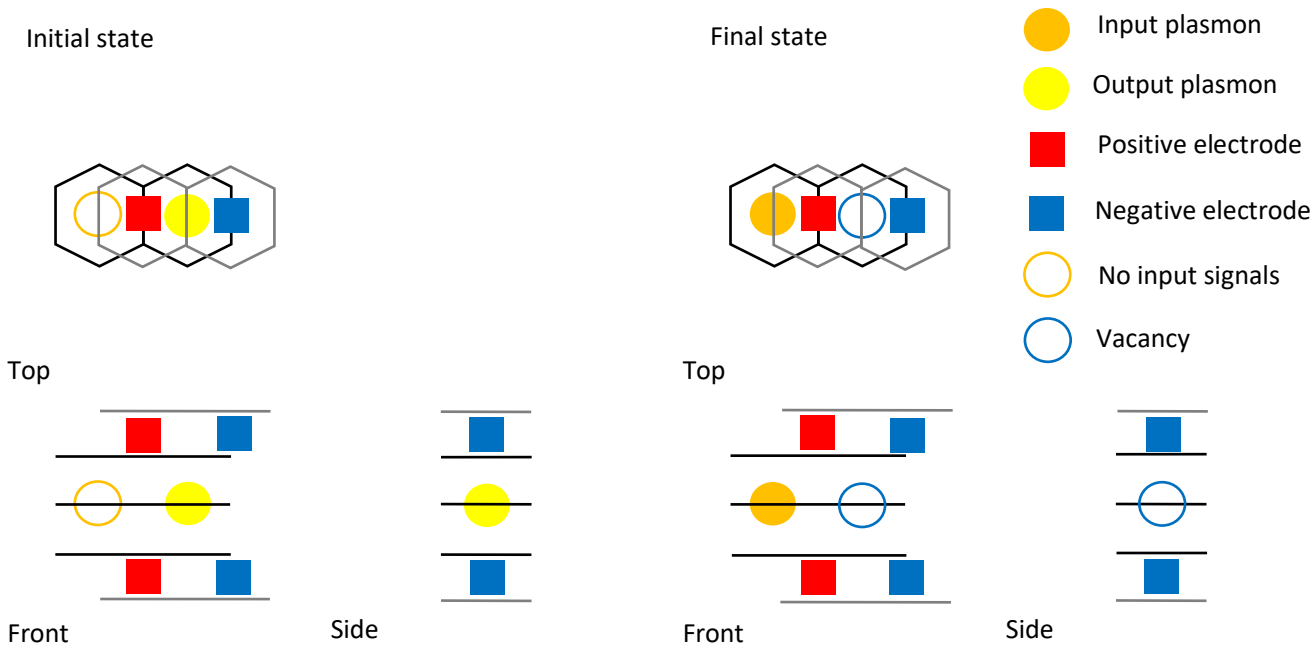


4. Hybrid architecture

1) AND and OR – A hybrid architecture that combines double AA stacking between double AB stacking. This architecture integrates both AND and OR logic within a single block. This concept is associated with the Combo gate described in the same paper discussed in Section 3 1). In the circuit design, the upper layers perform OR logic, while the lower layers execute AND logic. The diagram illustrates the effect of activating the OR layer, which causes the circuit to produce an output signal.



2) NOT – The NOT operation needs to be adapted for use the hybrid architecture. When input signals are coming, output plasmons generated by negative electrodes are drained to positive electrodes.



5. Discussion

1) Using THz technology, we could expect to generate plasmons at frequency exceeding 10 GHz, while simultaneously reducing overall power consumption compared to traditional electronic circuits.
2) With the ability to feedback output to input and dynamically change logic patterns, we could shrink the die size down to that of a programmable chip.
3) All components utilized in this system were designed so simple, making it relatively straightforward to manufacture them at the nanoscale level.
4) The exact mechanism by which logic can be produced using this component design remains to be studied, and will require further investigation.

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