Terahertz-Clocked Half Adder Using Graphene Plasmons as Bits

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Abstract: Next-generation computers have been researched worldwide, primarily focusing on quantum computers and alternative computing methods, as traditional semiconductor computing has reached its physical limits in terms of miniaturization, performance, and energy consumption. In this paper, we explore the design of a half adder as an example of a novel computing architecture. We utilize a terahertz-generated bit [1] to design logical patterns, building on prior work [2][3].

1. Introduction

To construct the half adder chip, we modified the original design from Fig. 1a (1) to the updated version in Fig. 1b. An additional graphene layer was placed below the original one, along with an Au bottom gate on the sapphire substrate. The top and bottom Au gates were finely segmented into lattices (Fig. 1c) and controlled via an electrode mapping controller to direct plasmon transport and interaction.

For logical computation in the half adder, the top and bottom Au gates were split into 72 segments each (Fig. 1c). Voltages applied to V_{Au1} (-1.2 V and 0 V) positioned the top graphene layer at its charge neutrality point (-1.2 V), blocking plasmon transport. Conversely, 0 V enabled plasmon propagation. For V_{Au2}, voltages of -2.4 V and -1.2 V generated plasmons in the bottom graphene layer. At -2.4 V, these plasmons inverted the behavior of the top layer's 0 V plasmons. Interaction between opposing plasmons resulted in annihilation, enabling NOT logic.

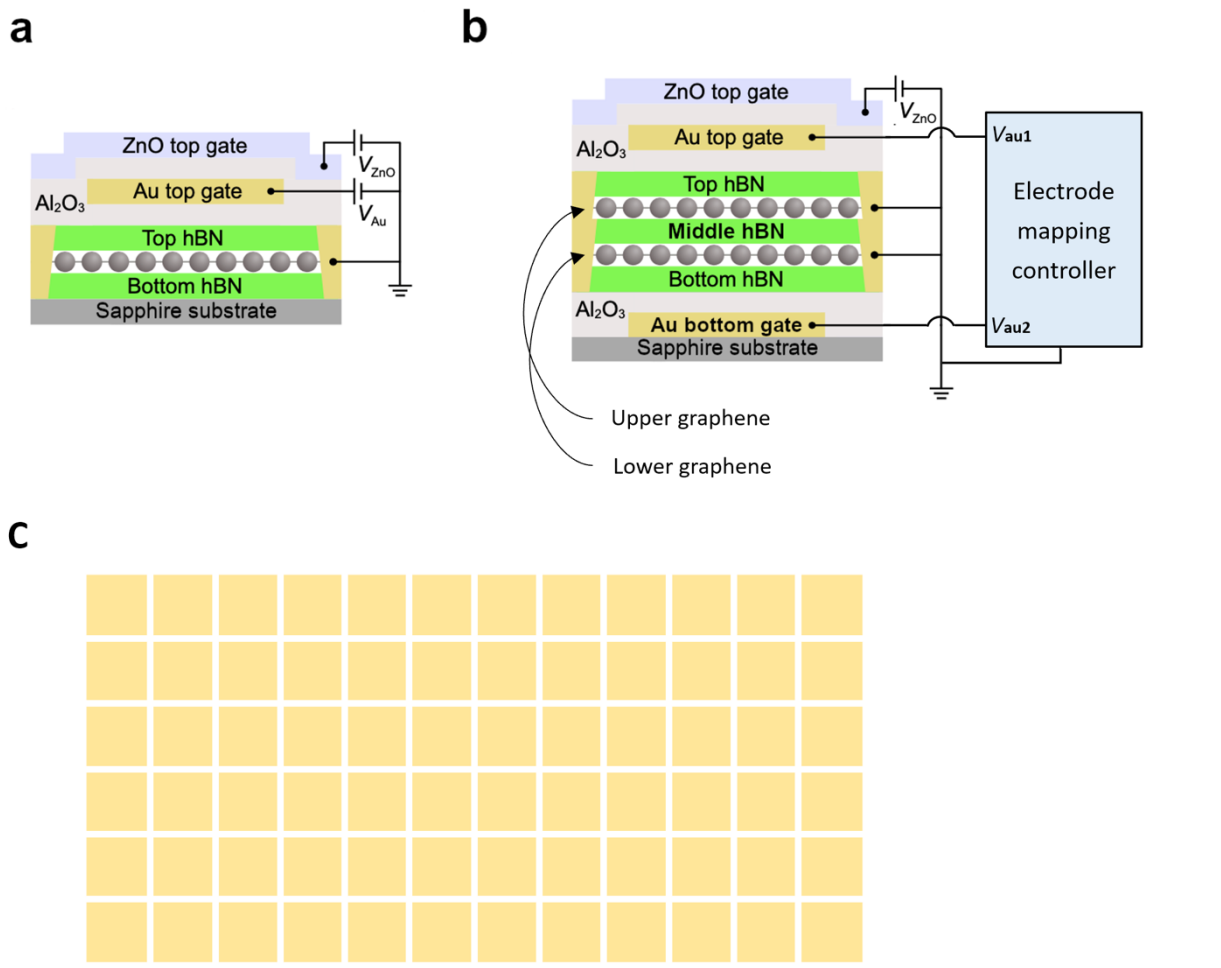


Figure 1 | Cross-sectional view of the half-adder chip. (a) Original design from Ref. (1). (b) Modified design with an additional graphene layer and Au bottom gate. (c) Overhead view of the latticed Au gates, controlled individually by the electrode mapping controller.

2. Half-Adder Logical Pattern Mapping

Fig. 2a illustrates the traditional half adder circuit (AND, OR, NOT). In Fig. 2b, the upper Au gate mapping routes plasmons (0 V = active path) for inputs A and B. Terahertz (THz) pulses enter from the left, process through graphene, and output Sum (S) and Carry (C). Fig. 2c shows the lower gate mapping, where a constant THz pulse generates inverse plasmons for NOT logic. At the NOT gate, opposing plasmons cancel, requiring precise phase alignment.

Plasmon paths are defined by gate voltage mapping, adjusted via parameters like path width, THz frequency, and voltage. This flexibility supports analog computing or hybrid digital-analog signal processing.

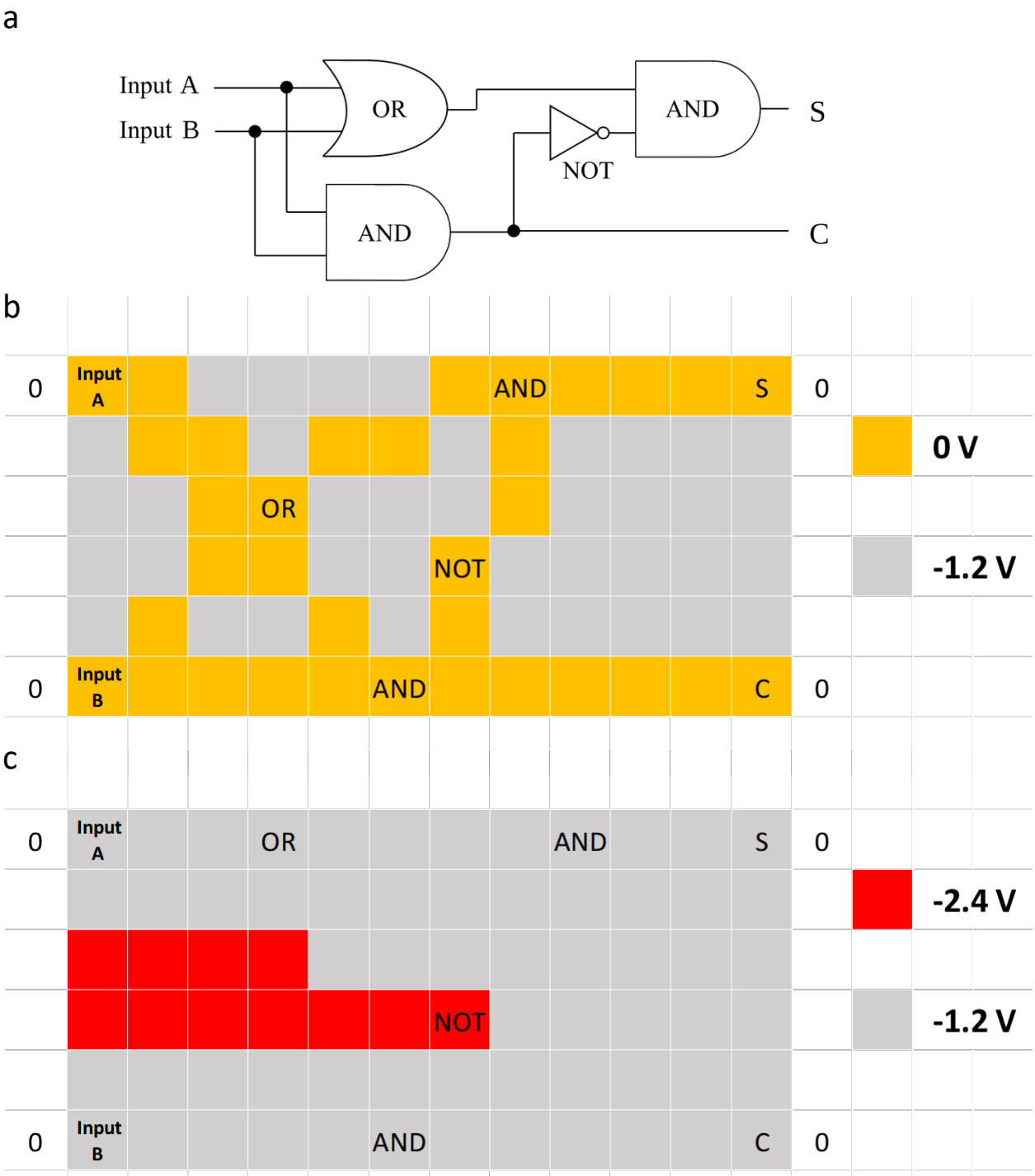
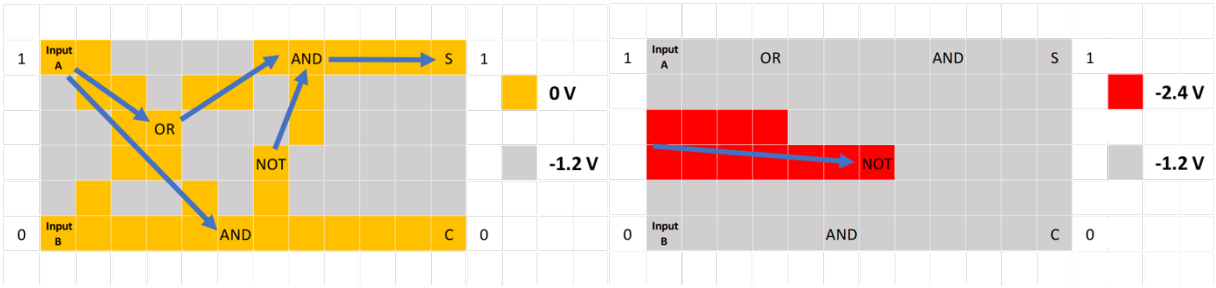


Figure 2 | Logical circuit and plasmon mapping. (a) Traditional half-adder logic circuit (AND, OR, NOT). (b) Upper Au gate mapping (inputs A and B at null). (c) Lower Au gate mapping for inverse plasmon generation (NOT logic).

3. Half-Adder Processing

Fig. 3 demonstrates plasmon behavior for three input cases:

a



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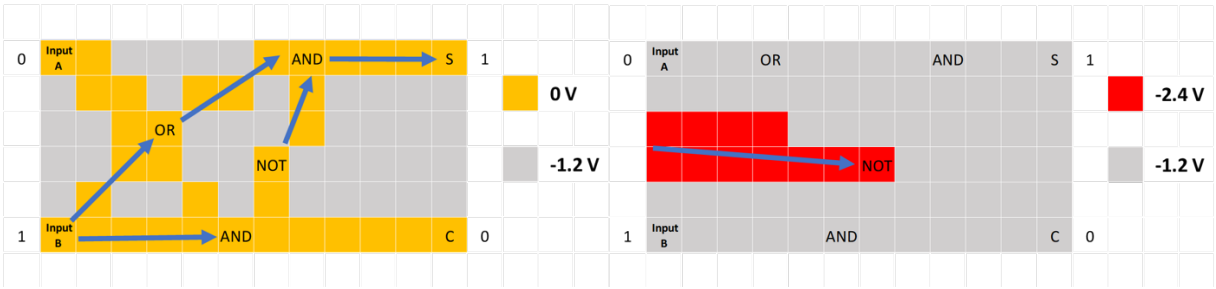

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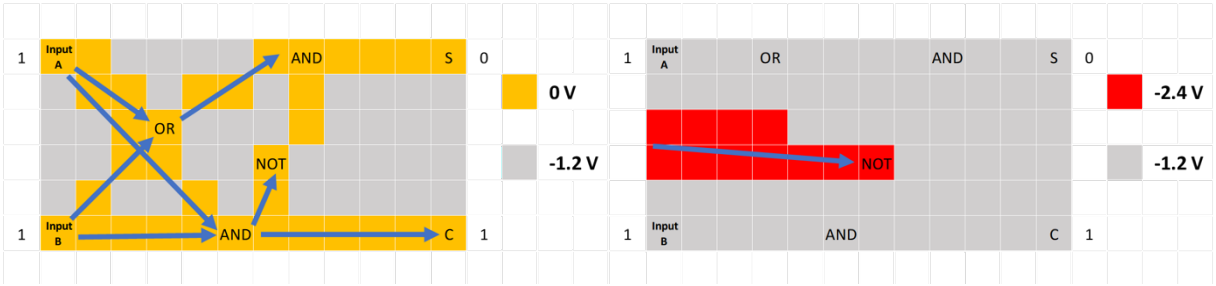

Figure 3 | Half-adder plasmon processing. (a): Input A=1, B=0. (b): Input A=0, B=1. (c): Input A=1, B=1. Outputs are derived from plasmon annihilation/transmission.

4. Discussion

This half adder design can scale to advanced architectures with terahertz clocks and low energy use. For AI applications, real-time feedback from outputs could remap gates, enabling simultaneous learning and inference. Multi-input/output configurations may support multitasking and compact, programmable chips.

References

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