The Fable Computer, Part IV: A Parametron of Pumped Resonant-Tunnelling-Diode Pairs

Phase logic below threshold at a 225-GHz carrier, with diode figures scaled from one published device; a 1-THz-class specification validated in the model only; and the one-pair experiment on which both rest

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Authorship and Status Disclaimer. This manuscript extends the author's design studies [1, 2, 3] ("Part I", "Part II", "Part III" throughout). Generation of content involved the use of an AI, Anthropic's Claude, at the author's direction. The model, its runs and this manuscript were prepared in a maintainer-operated Claude Code session in November 2026, whose main thread ran on Claude Fable 5.1 and Claude Fable 5.2 and whose agents all ran on Claude Opus 5.5. The agents were a theory reader, readers of the literature, checkers of the references at their primary sources and the writers of three further codes of the same circuit. Others read Parts I to III, and built and checked the outline of this Part. Others wrote and checked the model's equations, investigated a disagreement between two of the codes, and checked the study's report and the note that corrected it. Others built and tested the code package and checked this text, which the main thread drafted. Appendix RB lists them and what they found. The circuit model of this Part is not one of the released model chains of Parts I to III and does not extend them. The author declares a lack of formal expertise in resonant-tunnelling-diode devices and in terahertz circuit design, and the document has not received independent expert review. All physical claims are results of that circuit model ("in-model": computed by the model of this Part under stated assumptions, not measured) and must be treated as a starting point for discussion, not as peer-reviewed engineering guidance.

Names. "The pair" is the element of this Part: two resonant-tunnelling diodes (RTDs) on one centre-tapped inductor. "The fabric of pairs" is the technology built from it. The single word "fabric" stays with the graphene-plasmon fabric of Parts I to III. "The 225-GHz design" is the pair and its clocking at a 225-GHz carrier. "The 1-THz-class cell" is the same design with every time, capacitance and inductance divided by 4.78; its carrier is 1.075 THz by name and 1.076 THz as run. The name "the Fable Computer" is extended here to this fork of the series, which has no graphene and no plasmon (Section 1.4).

Labels. Every statement that is not a definition or plain arithmetic carries one of these labels.

- **in-model**: a run of the RTD circuit model of this Part. Where a sentence also speaks of Parts I to III, the label names the model: "in-model (RTD circuit model)".
- **design**: a choice of this Part, not a result.
- **external**: a maker's or literature value, with its reference. Where a source was read below full text, the level is given, as in "(external, abstract)".
- **this paper's arithmetic**: a calculation on stated values.
- **open**: unsettled.
- **prediction, conditional**: the outlook of Section 12 only.
- **demonstrated (runnable)**: a check that a listing of the code package performs on the code. It is never a physical statement.

A statement of Parts I to III is given with its section and, where it has one, with the label it carries there, as in "(Part III, Section 5.2; in-model there)". A count of zero is a count and not a rate. Every count is given with its number of runs, with the spreads it carried and with its noise level. "Validated" is used only as "validated in the model".

Abstract

Part I notes that terahertz electronic oscillators such as resonant-tunnelling diodes (RTDs) "exist but lack a restoring, cascadable logic family at those frequencies" (Part I, Section 2). This Part asks whether RTDs can be that family, in a circuit model outside the released model chains of Parts I to III. The element is a pair of RTDs on a centre-tapped metal inductor, biased just below its own oscillation threshold and pumped at twice its carrier frequency (design). In the model the pair is silent without the pump. With it the pair settles on one of two phases half a turn apart, within about 10 ps after a seed is removed at the design's supply level. That phase

is its bit, as in a parametron (in-model, one pair alone). Two published RTD sources, at 450 and 320 GHz, cannot pump a 1.075-THz cell, which needs 2.15 THz; each sets a slower design at half its frequency, and neither is the pump of that design as built (external; design). The 225-GHz design scales its diode from the first; its delay, its contact and the shape of its curve are assumed (design). At the noise of that design, with a 25 % pump and a 3 % inductance spread, a row of sixteen holds at the eleven supply levels run from 0.880 to 1.030 V (in-model, two codes; 32 runs per level in this Part's model and 8 in the second). At 0.94 V and that noise, adders of 53, 106 and 169 pairs, a serial adder and an eight-bit accumulator give no wrong result in 32 runs each, without spread and with an inductance spread of 3 or 5 % (in-model, in one code; the serial adder with the 3 % spread also in a second; counts, not rates). With nine spreads at once, whose pump phase error is 10 degrees, the four-bit adder errs in 5 of 256 draws at that noise and in 7 of 256 at 4.78 times that noise power; the accumulator, with 32 draws at that noise, errs in 2 (in-model, in one code; counts). Without spread, a row of sixteen, the four-bit, eight-bit and serial adders and the accumulator show no wrong decision at 16 times the design's noise power, in 64 or 127 runs each. At 64 times the eight-bit adder and the accumulator each show one wrong result in 64 runs, and at 128 times every layout with logic fails (in-model, in one code; counts; full shot noise assumed). Three further codes written from specifications find the same range of free oscillation of one pair, and two of them its two pumped phases. Within the lines each ran, with a 3 % inductance spread, they agree with this Part's model on the serial adder except at 0.880 V and at a 40 % pump at either noise level, and at 1.015 V at the higher one. Those differences, and others in two four-bit adder lines and two row lines, are unexplained. All other results rest on one code (in-model). The same design with every time, capacitance and inductance divided by 4.78 is a 1-THz-class cell: carrier 1.075 THz, slot 14.5 ps, junction 0.52 fF, diode delay 21 fs (design). The step is a change of units, exact for the model's equations, in which the noise power against the signal rises 4.78 times (this paper's arithmetic). At that higher noise, with a 3 % inductance spread, the four-bit and serial adders lose at most one step of each working range and fail more often at their edges (in-model; some serial-adder lines also in other codes; 32 or 16 runs per line; counts). The specification is validated in the model only, and there within the lines run. That cell asks 3.3 to 5 times the peak current per capacitance of the fastest published diode, and its contact is at or beyond the edge of what is reported (this paper's arithmetic; external). The pump needs about 0.1 mW per pair at 2.15 THz, where a source on a chip gives 0.6 µW at 2.06 THz. Pump, clock, inputs and outputs are ideal in the model (this paper's arithmetic; external; open). A pair takes 7.2 mW, or 0.50 pJ per slot at 225 GHz and 0.10 pJ in the 1-THz class, before the pump (in-model; this paper's arithmetic). If one pair works in hardware, and if such diodes, pump sources at twice each carrier and their efficiency exist, a scaling rule at fixed voltages would lower that energy until noise ends it between 31 and 8 fJ, in runs without spread and with full shot noise assumed (prediction, conditional). Four experiments would falsify the scheme, and the first decides: one pair below its threshold, pumped at twice its frequency. For a 160-GHz pair it needs 0.01 to 0.06 mW of pump power, about the 40 µW at most of the second source, if most of that reaches the pair (in-model; this paper's arithmetic; external). Nothing has been built, and a literature search found no RTD reported to oscillate on two set phases at half a pump frequency (external).

1 Introduction

1.1 The question

Part I designed a terahertz logic fabric whose gain cell is a graphene channel with a drift current. In its survey of competing platforms it notes that terahertz-capable electronic amplifiers and oscillators, among them resonant-tunnelling diodes, "exist but lack a restoring, cascadable logic family at those frequencies" (Part I, Section 2). Its table of platforms lists RTDs as "latch only". Part I also leaves open which compact source should supply its carrier, with "a resonant-tunneling diode" named among the candidates (Part I, Section 3.2; open there). And of an electrical gain stage that its machine would need if an inversion uses the gate-segment route, it says: "Its device class and placement, and the class of the clock source, are open design questions, tracked as issues #141 and #139" (Part I, Section 9.8).

Part IV asks the question that these passages leave: can RTDs themselves be the logic family? It answers with a circuit model. The element is a pair of RTDs on a metal inductor. The pair is biased just below the level at which it would oscillate by itself and is pumped at twice its oscillation frequency. In the model it then oscillates on one of two phases half a turn apart, and that phase is its bit. An element of this kind is a parametron [18, 20].

Nothing has been built, and a literature search found no RTD reported to behave in this way (external; a literature search).

1.2 The requests behind the study, and the plan of the paper

The study began with a narrow request from the maintainer. An earlier, unreleased trial of this project had used a pumped pair at a 1.075-THz carrier, which needs a pump at 2.15 THz on the supply of every pair. Could a 450-GHz source built of RTDs by Canon [4], paired with a 320-GHz RTD device from ROHM [5], do that job? A second request widened the task: take every completed trial into account and build a design that computes, with those devices or with RTD specifications that do not exist yet, leaving power and cost aside. A third asked for this Part: models with existing RTDs first, then a specification for the 1-THz class and, if that specification is validated, which here can only mean in the model, a brief prediction of where the approach could lead.

The paper follows that order. Sections 2 to 10 treat the two sources and the design at a 225-GHz carrier that follows from them. Section 11 gives the specification for the 1-THz class and says in what sense it is validated: in the model, and in no other sense. Section 12 gives energy and throughput and a conditional outlook of at most a few hundred words. Section 13 states four experiments that would falsify the scheme, Section 14 lists what is not shown, and Section 15 concludes.

1.3 In what sense the RTDs are existing ones

No existing diode is used as it is. The pump frequency of the 225-GHz design is that of one published source, Canon's array at 0.45 THz [4]. The currents and the capacitance of the diode are scaled to a quarter of the per-device figures of that source, whose diode area is not published (design; external). The diode's delay, its contact resistance and the shape of its curve between peak and valley are assumed (design). Section 5 gives every value with its kind, and Section 10 varies the assumed ones.

1.4 A fork in the device

Part II called its cold temperature classes "a fork from Part I's charter, not a refinement of it" (Part II, Section 1). Part IV is a fork of another kind, in the device. It has no graphene and no plasmon. It changes no number of Parts I to III. It uses three of their results as yardsticks and four as comparisons: a booked power (Section 4), the energy entries of Part I's Table 1 and Section 8.1 (Section 12.2), and Part II's crossover temperature (Section 9.7). It claims none of them. Other statements of those Parts are quoted as related work or for scale, not as support. It keeps their rule of no cryogenics: the noise of the model is that of 353 K. The name "the Fable Computer" is extended here to this fork. The project's question was stated for a graphene-plasmon fabric, and Part IV lies outside that statement.

The second request set power aside, and the paper still reports it. The reason is that power decides whether a source can pump a pair at all (Section 2), and that energy and heat bound the outlook (Section 12).

1.5 The three weakest points

They are stated here so that no later section is read without them.

- **The effect itself is unreported.** A search of the literature found no RTD oscillator that is pumped at twice its frequency and settles on one of two set phases. The nearest report is a frequency divider by two made of RTDs and transistors that operated at 88 GHz [26] (external, index abstract). One pumped pair in hardware decides whether the scheme exists (Section 13).
- **The pump is not designed, and its source does not exist near 2 THz.** The pump, the clock, the inputs and the outputs are ideal sources in the model. The 1-THz-class cell needs about 0.1 mW of pump power per pair at 2.15 THz (this paper's arithmetic). The highest powers found from a chip between 1.9 and 2.1 THz are 0.6 μW in continuous operation at 2.06 THz [34] and 0.4 μW at 1.92 THz ([8], abstract; the power from the thesis [13], secondary, and not stated as continuous) (external). That is about 170 to 250 times short (this paper's arithmetic).
- **With the full set of nine spreads the four-bit adder fails in a few per cent of the draws.** Nine spreads of the parts were drawn together at the sizes of Section 8.5, with a pump phase error of 10 degrees. A four-bit adder of 53 pairs then gives a wrong addition in 7 of 256 draws at the noise of the 1-THz-class cell and in 5 of 256 at the noise of the 225-GHz design (in-model, in one code; counts, not rates). The accumulator,

with 32 draws at the noise of the 225-GHz design, has 4 wrong words of 128, in 2 of the draws (in-model, in one code; a count, not a rate). No layout larger than 53 pairs was run with enough draws to size a machine of thousands of pairs. If pairs failed independently at the four-bit adder's rate, a machine of 10,000 pairs would be right in 0.6 and 2.5 % of builds at the two noise levels. Those are point estimates: by the 95 % intervals of that rate the share lies between about 0.003 % and 30 % (this paper's arithmetic).

2 The two sources

2.1 The answer

Neither device can serve as the 2.15-THz pump. A pump of this kind must run at exactly twice the carrier and in step with it. For a carrier of 1.075 THz that is 2.15 THz. Canon's source runs about 4.8 times lower and ROHM's 6.7 times lower (external; this paper's arithmetic). Multiplying either source up to 2.15 THz was not assessed.

They cannot serve as pump and carrier for each other either. 450 GHz is 1.41 times 320 GHz, not twice. Their sum and difference, 770 and 130 GHz, serve nothing here.

Each defines a slower design of its own. A pump defines a carrier at half its frequency, and the slot then follows from the number of carrier periods that a decision is given. This Part keeps 15.6 periods (design).

Table R1. Pump, carrier and slot. A slot is one clock period of 15.6 carrier periods.

Pump	Carrier	Slot	What the source offers (external)	Reading in this Part
Canon's array, 450 GHz [4]	225 GHz	69 ps (14.4 GHz)	11.8 mW from 72 RTDs locked to each other on one chip	the 225-GHz design of Sections 5 to 10
ROHM's device, 320 GHz typical [5]	160 GHz	97 ps (10.3 GHz)	40 µW at most from one packaged RTD device	one pair at most: a first experiment (Section 13), not a fabric of pairs
none found	1.075 THz	14.5 ps (69 GHz)	the highest RTD fundamental found is 1.98 THz, with no power reported for it ([6], through [7] and [14])	the 1-THz-class cell of Section 11, which stays without a pump source

2.2 Canon's array

All of this is external, from one paper that is open access and was read in full by two readers of this study [4].

- **What it is.** An array of 36 patch antennas on a chip of 3.2 mm by 3.2 mm, each with two RTDs. It radiates 11.8 mW at 0.446 THz from 1.12 W of supply power, about 1 %. That is about 0.32 mW per antenna.
- **The two RTDs of a patch run in antiphase.** The node of the field lies at the centre of the patch, where the supply enters. This is the balanced pair of this Part, built 36 times and locked by coupling lines, for radiation and not for logic. Canon's pairs run above their own threshold and are not pumped.
- **One feed line serves all antennas.** No antenna is biased or switched by itself. The paper proposes separate feed lines per antenna and does not show them.
- **The diode.** The mean peak current is 25.4 mA, with a three-sigma spread of 0.2 mA over three RTDs of one chip and of 1.6 mA between two chips 20 mm apart. The drop from peak to valley, 14 mA over 0.55 V, is fitted to a cubic curve, because the measured curve has a plateau and shows no valley. The capacitance, about 10 fF, is fitted from the oscillation frequency. The diode area is not given.
- **Locking.** The paper gives the tolerances within which a small array locks: 18 % in amplitude, 9 % in phase and 1.5 % in frequency. It shows no locking to an outside reference and no control of the phase.

2.3 ROHM's device

All of this is external, from the maker's release and the presentation linked from it, both read in full [5]. The maker calls it an RTD device. Its chip is 0.5 mm by 0.5 mm, in a package of 4.0 mm by 4.3 mm. It gives 40 µW at most, at a typical frequency of 320 GHz, from a typical consumption of 40 mW, without cooling. An evaluation kit has been sold since August 2026. The maker's roadmap shows a third generation at 450 GHz and above, under development. Such a device would have the pump frequency of the 225-GHz design.

A ROHM prototype at 322 GHz gave about 8 µW, with a linewidth of 4.4 MHz at half width when it ran free [29]. RTDs made by ROHM have been locked to a signal at their own frequency [30]. An RTD has been shown

to lock in antiphase to an injected pulse, with the locked signal building up in about 50 ps [31] (external). Locking of such a device at half or at twice its frequency was not found.

2.4 What the pump of a fabric of pairs would take

In the model the supply source of one pair carries a pump term of 235 mV and passes 6.1 mA of pump current, almost all of it reactive (in-model, one pair alone; Section 6). Through a resonant feed with a quality factor of 5 to 10 that costs 0.07 to 0.15 mW of real pump power per pair (this paper's arithmetic, not a design). Towards the low end of the supply range the pair itself absorbs pump power as well: 0.05 to 0.07 mW at 0.88 V with a pump of 25 to 30 % (in-model, one pair alone). Canon's chip radiates about 0.16 mW per RTD (external; this paper's arithmetic). So a pump plane would need about one pump RTD per logic pair (this paper's arithmetic).

Canon's chip as built is not that pump plane. As its paper describes it, the chip radiates its power; delivery of that power to supply nodes was not searched for. It has one feed line and so no separate clock phases, and the paper shows no locking to an outside reference (external). The design of Sections 5 to 10 takes from it a frequency, a diode and the fact that a balanced pair of RTDs fed at its node has been built.

A single pair tuned to a 160-GHz carrier and pumped at 320 GHz was also run. It oscillates on two phases with a pump of 10 % from a supply level of 0.94 V, and with 15 % from 0.91 V (in-model, one pair alone). By the same arithmetic such a pump takes 0.01 to 0.06 mW. That is about the 40 μW of ROHM's device, if most of that power reached the pair (this paper's arithmetic; external). ROHM's device could therefore pump one pair at most. Section 13 makes that pair the first experiment.

3 Related work and positioning

The parametron. Phase logic with an oscillator driven at twice its frequency is from the 1950s. Goto's parametron oscillates at half its driving frequency and holds a bit as one of two phases half a turn apart [18] (external, abstract). Von Neumann's patent of the same years describes majority organs of three or five inputs, conjunction and disjunction by a permanent source, and supplies modulated in three phases [20] (external, patent text). Parametron computers had 4,200 and 13,000 parametrons, majority gates, inversion by a reversed winding and three excitation phases [19] (external, a secondary source). A microwave version ran a 3.7-GHz pump and 1.85-GHz logic with a balanced varactor circuit and a three-phase supply [21] (external, abstract).

A tunnel-diode pair of 1961. A patent with British priority of March 1961 describes a circuit that is very close to the pair of this Part [22] (external, patent text, partly hidden in the scan). Two tunnel diodes sit in series, the bias enters at the junction of a split inductor, and a drive at twice the resonance is applied across the pair. The bit is the phase of the oscillation. Majority inputs and two or three drive phases along a chain are described. The circuit is quiescent without the drive, and most of its output power comes from the supply. This Part therefore does not claim the topology, the majority gate, the clocking in phases or the gain from the supply as new.

What differs from that circuit. There the diodes switch between their two positive-resistance branches, as a large-signal switch, at a drive of 250 megacycles per second. Here the pair is an RTD pair held just below its small-signal oscillation threshold, at hundreds of gigahertz. What this Part adds is a circuit model of that RTD version with its tolerances, with stored state and with the region of diodes for which it works. Whether the older circuit could be biased in the same way was not checked. Three design choices distinguish this design from the earlier trials of this project, of which the first is not new: the bias below threshold, the input aligned with the pump, and the pump step of three quarters of a turn with one inversion per loop. The first is the regime of the parametron and of the circuit of 1961, both quiescent without their drive. Whether either used the third was not checked.

Series pairs of negative-resistance devices on a clocked supply. Two earlier logic families use a series pair of negative-resistance devices on a clocked supply, and both have been built. In the tunnel-diode "twin" of Goto and co-workers two Esaki diodes sit in series. A bit is the polarity of the potential at their mid-point, that polarity is set by the majority of the inputs, and groups of twins are energised one after another in three phases. A clock of 30 megacycles per second is reported, and the authors call the principle similar to that of the parametron [39] (external, abstract). In the monostable-bistable transition logic element (MOBILE) of Maezawa and Mizutani, two negative-resistance devices in series are driven by an oscillating bias through a transition from one stable state to two, which allows a large fan-out [40] (external, abstract). Threshold gates of

three weighted inputs were shown with it [41] (external, abstract). MOBILE gates of RTDs and transistors have run at up to 35 Gb/s [42] (external, abstract), and the title of one report names operation at 100 GHz [43] (external, index record). In the abstracts read, the bit of the twin is the polarity of a potential at its mid-point [39]; whether a twin is ever run as an oscillator is not in that abstract. No abstract of the MOBILE states how its bit is encoded, and that it is a level is an inference from its bistable output. None of them mentions a carrier or a pump at twice a carrier. If the full texts agree, the phase of a pumped carrier is the difference from the pair of this Part. The series pair, the majority at its mid-point, the supply clocked in phases and a latching RTD gate with fan-out are therefore not new here. Part I's sentence on RTDs, quoted in Section 1.1, speaks of terahertz frequencies. The 30 megacycles per second of the twin lie far below every rate of this Part. The 35 Gb/s of [42] lies above the 14.4-GHz clock of the 225-GHz design and below the 69-GHz clock of the 1-THz-class cell. The 100 GHz named in the title of [43], whose meaning was not read, lies above both. Those clocks are modelled, not built.

Phase logic with oscillators that run by themselves. A recent line of work builds phase logic from self-sustaining oscillators that are locked by a signal at twice their frequency [23, 24] (external). There the oscillator runs with or without that signal, and the signal only makes its phase two-valued. In Section 6 a pair biased above its threshold behaves in that way, and it is slow to settle (in-model). This Part follows the older case of Goto and von Neumann: the pair is silent without the pump.

RTD circuits at half or twice a drive. No RTD oscillator pumped at twice its frequency with a two-valued phase was found, and no parametric oscillation of an RTD. Two reports come nearest. A dynamic frequency divider by two, made of RTDs and transistors, operated at 88 GHz [26] (external, index abstract; the abstract does not say whether 88 GHz is its input or its output). Its RTD circuit has been called a kind of van der Pol oscillator with an input terminal [27] (external). It is driven at twice its output, as the pair is, but no report of its two output phases being set or used was found. In the other report an RTD oscillator at about 550 GHz is locked by a signal at half its frequency, which is the opposite case [28] (external).

Locking data near 1 THz. Part III reports a check that "found no injection-locking or phase-noise data for resonant-tunnelling diodes at 0.8–1.2 THz" (Part III, Section 8.1(e); external there). The 1-THz-class pair of Section 11 would have to lock at half a 2.15-THz pump. This Part found no such data either.

The superconducting parametron. Part I sets superconducting single-flux-quantum logic aside by its rule of no cryogenics, naming it "with its adiabatic AQFP variant" and citing a paper on the former (Part I, Section 2). That variant, the adiabatic quantum flux parametron, is reported in [25], which this study did not read. Part IV keeps the rule and uses no figure of that technology.

4 What Part IV keeps, changes and sets aside

When Part IV takes up a construct of Parts I to III, it keeps it, changes it or sets it aside (Table R2). It keeps the question of the series, whether the machine computes, and the discipline of labels. It keeps the rule of no cryogenics and takes 353 K as the temperature of its noise, the cap of the series. It keeps three results of the earlier Parts as yardsticks, with their labels, and claims none of them. The first is the pass line of 6.3×10^{-9} per cell decision (Part III, Section 5.2; in-model there, an upper bound). The second is the length of 92 cells of Part III's critical path, used here only as a row length (Part III, Section 4.3; in-model there). The third is the slot of 14.5 ps, which Part III uses at a frontier of 69 GHz that is "neither confirmed nor moved (open)" (Part III, Section 2.2). Part IV also sets the power of a pair beside the cell dissipation that the released chain books (Section 12.2). Section 12.2 further sets the pair's energy per slot beside the energy entries of Part I's Table 1 and Section 8.1, and Section 9.7 sets its quantum temperature beside Part II's 48 K. Four changes are substantive.

- **The gain element.** An RTD pair on a metal inductor replaces the graphene cell with its drift current. Part IV makes no statement about that cell.
- **The bit.** The bit is the phase of an oscillation, not the presence of a pulse. Parts I and II studied a cell pumped at twice its carrier and found that it "restores phase in a narrow window", with knee-level swings under a 5 % pump and "only weakly at the delivered '1'" (Part I, Section 5; in-model there). Those are results for another device. They are related work for Part IV and not support.
- **State.** Part III's lane has "no registers; nothing held on the fabric between slots" (Part III, Table T2). Part IV holds state on the fabric of pairs, in loops of four pairs. That is a declared change of design.

- **The clock.** Part I's timing is optical, because for its graphene bias plane "no electrically modulated clock is physically available" (Part I, Section 1). Part IV's clock is electrical, has four phases and switches the supply of each pair. It is ideal in the model. Whether a supply and clock plane can deliver it, at 14.4 GHz with edges of 14.3 ps or at 69 GHz with edges of 3 ps, is open.

Table R2. What Part IV keeps, changes and sets aside.

Construct	Parts I to III	Part IV	Set aside in this study
Gain element	a graphene cell with a drift current, biased below its instability	a pair of RTDs on a centre-tapped metal inductor, biased below its own oscillation threshold (design)	a graphene tank at 320 GHz; a diode tuned by graphene; a pair biased above its threshold, where the pump only steers
The bit	a pulse, present or absent. "In the design model of Section 5, logic levels are restored at every gate by saturating regenerative gain, and inversion is a bias choice. The released model qualifies both" (Part I, abstract)	one of two phases half a turn apart, set by a pump at twice the carrier (design)	one diode with on/off keying
Logic	threshold cells in the design model; in the released model "the cell compresses, it does not threshold" (Part I, Section 5; demonstrated there); under a phase encoding a majority that "reads the sign of the summed field", admissible only for inputs of a third of the knee or less, "far from decision grade" (Part I, Section 5; in-model there)	majority of three; AND and OR by a held input; inversion by a reversed link or by a choice of rail (design)	interference gates without restoration
State	"no registers; nothing held on the fabric between slots" (Part III, Table T2)	a loop of four pairs keeps a bit (design; in-model, Section 8)	none
Clock	optical; "no electrically modulated clock is physically available" for the graphene bias plane (Part I, Section 1)	electrical, four phases, ideal in the model (design; open)	a pump phase that steps by half a turn per clock phase
Slot	14.5 ps, at a frontier of 69 GHz that is "neither confirmed nor moved (open)" (Part III, Section 2.2)	69 ps in the 225-GHz design; 14.5 ps in the 1-THz-class cell, equal by choice (design)	none
Temperature	"no cryogenics, and chip temperature ≤ 80 °C" (Part I, abstract)	no cryogenics; noise at 353 K; the cap is neither met nor tested (Section 12)	none
Power per element	12.67 µW booked per cell at the 353 K cap at the hydrodynamic tier, with an upper bound of 16.64 µW, on Part I's best-case lifetime (Part III, Section 2.2)	7.2 mW per pair, before the pump (in-model; Section 12)	none
Decision error	a pass line of 6.3×10^{-9} per cell decision (Part III, Section 5.2; in-model there, an upper bound)	counts of wrong decisions in runs; no rate is claimed against the pass line	none

The entries of the last column are unreleased work of this study. They are named so that a reader knows what was tried and left. No result of them is used, except that Section 6 shows a pair biased above its threshold for comparison.

5 The cell, the clock and the model

This section specifies the element closely enough for a reader to rebuild it. Sections 5.1 to 5.4 are design. Section 5.5 gives the model in which every later result is computed.

5.1 The pair

Two RTDs share one supply node. Each feeds one end of a metal inductor whose centre tap is grounded, and a metal capacitor at each end sets the frequency (Figure R1(a)). The pair oscillates with its two ends in antiphase. The bit is the sign of that oscillation against a reference at the same frequency.

The pair is biased just below the supply level at which it would oscillate by itself. A pump at twice the carrier frequency is added to the supply voltage, at a quarter of its level. With the pump the pair oscillates, and only on two phases half a turn apart (in-model; Section 6). Those two phases are the 0 and the 1. The line through them in the plane of the two quadratures is called the pair's axis.

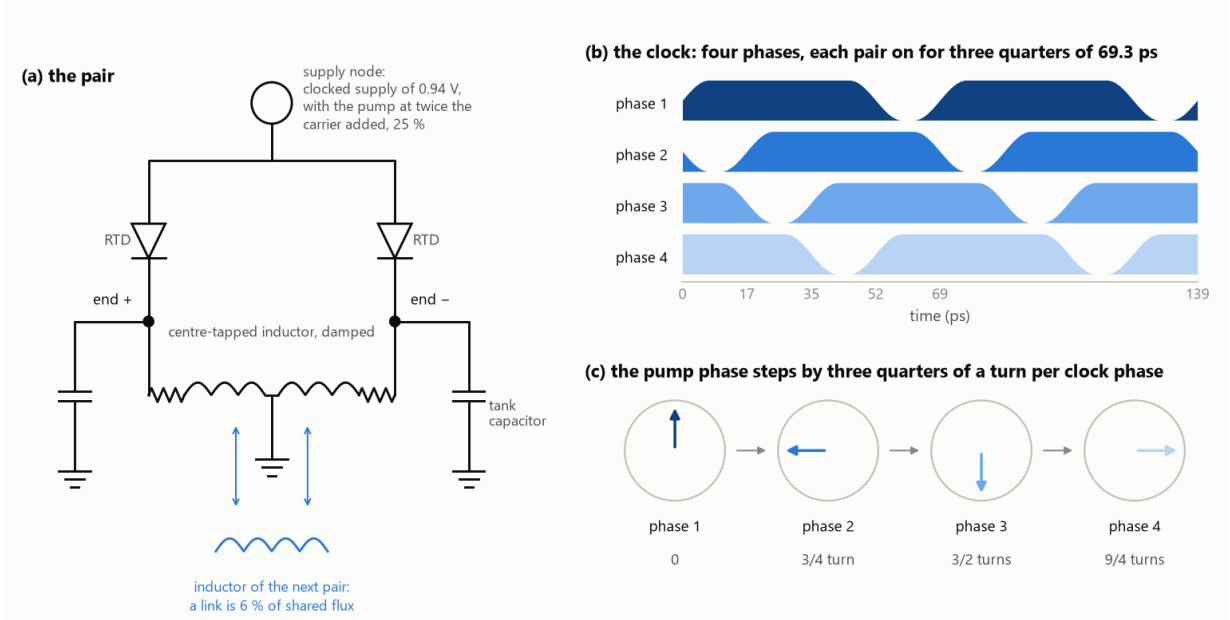


Figure R1. The design (no result is plotted). (a) The pair: two RTDs on one supply node, a centre-tapped and damped inductor, a tank capacitor at each end; a link to another pair is a small mutual inductance between the two inductors. (b) The four-phase clock of the 225-GHz design: each pair is on for three quarters of a period of 69.3 ps, and a pair takes its sign from the pairs switched on a quarter period earlier. (c) The pump phase steps by three quarters of a turn from one clock phase to the next.

5.2 The cell in numbers

Table R3 gives every value of the cell with its kind. The diode figures are a quarter of the per-device figures of one published source [4], whose diode area is not published. Its delay, its contact and the shape of its curve are assumed. The 1-THz-class cell of Section 11 is the same circuit with every time, capacitance and inductance divided by K = 1.075/0.225 = 4.78.

Table R3. The cell. “Design” marks a choice of this Part, “assumed” a value for which no measurement was found, “in-model” a result of the model.

Quantity	The 225-GHz design	The 1-THz-class cell	Kind
Diode currents, per diode	peak 6.35 mA, valley 2.85 mA, 0.55 V between them	the same	a quarter of the fitted figures of [4] (external; design)
Junction capacitance, per diode	2.5 fF	0.52 fF	2.5 fF is a quarter of the fitted 10 fF of [4]
Diode delay	100 fs	21 fs	assumed
Contact resistance, per diode	12 Ω	12 Ω	assumed
Tank, per half	16 fF, of which 13.5 fF is a metal capacitor; 26.3 pH in the antiphase mode	3.35 fF; 5.5 pH	design
Inductor	centre-tapped; coupling of the two halves 0.3; 9.3 Ω in series with each half, for a quality factor of 4	the same resistance	design; the damping is deliberate
Supply source	2.5 Ω, with 4.78 fF on the supply node	2.5 Ω, 1.0 fF	design
Oscillates by itself	from 0.97 to 1.14 V	the same	in-model
Supply level	0.94 V	0.94 V	design
Pump	450.4 GHz, 25 % of the supply level: 235 mV	2.152 THz, 25 %	design
Carrier	225.2 GHz	1.076 THz	half the pump
Clock	period 69.3 ps (14.4 GHz); four phases; on for 0.75 of the period; edges of 14.3 ps	period 14.5 ps (69 GHz); edges of 3 ps	design: 15.6 carrier periods per slot
Link	a mutual inductance of 6 % of the pair’s own, 1.58 pH in magnitude	0.33 pH in magnitude	design
Input	a current of 0.4 mA at the carrier, aligned with the pump’s axis	the same	an ideal source
Direct current and power	10.5 mA per pair while on; 7.2 mW per pair on average	the same	in-model

5.3 The clock, the pump step and the links

The clock has four phases. A pair is on for three quarters of a period, and the supply of each pair rises and falls over 14.3 ps (Figure R1(b)). A pair takes its sign from the pairs that were switched on a quarter period before it. One hop from pair to pair therefore takes a quarter of the period, 17.3 ps. A slot is one period: every pair takes one decision per slot.

The link between two pairs is a small mutual inductance between their inductors, 6 % of the pair's own inductance. The design has no other coupling between pairs. Section 8.6 shows what a stray capacitance between pairs costs.

The pump phase steps by three quarters of a turn from one clock phase to the next (Figure R1(c)). The reason is the phase of the link. An inductive link delivers its seed turned by more than a quarter turn against the pair that sends it. With a step of three quarters of a turn of pump phase, which is three eighths of a turn of carrier phase, the seed lands close to the axis of the pair that receives it. A linear analysis by a theory reader of this study, made before any run, put the best step near 250 degrees of pump phase (an analysis, not a run). Of the steps that a loop of four pairs allows, the multiples of a quarter turn, three quarters is the nearest (design). One consequence follows for loops: a bit carried once round a loop of four pairs comes back inverted. Every such loop therefore holds one inversion: a reversed link on one rail, or a crossing of the two rails in the dual-rail form of Section 5.4.

All paths into a gate have the same number of hops. Rows of buffer pairs make up the difference, as delay cells do in Part I.

5.4 Logic and state

A pair with one input copies it. A pair with three inputs takes their majority, because the three seeds add on its axis and the pump lets only the sign of the sum grow. With one input held at 0 or at 1 a majority is an AND or an OR. An inversion is a link of the opposite sign, which at this size is a twist in a coupling loop. Where every link must have one sign, every bit travels on two pairs, as itself and as its complement, and an inversion is a choice of rail. Both forms were run; they are called single rail and dual rail below.

A stage of a ripple-carry adder has five pairs, three of them majority gates (Figure R2(a)). With inputs A, B and carry C, the carry out is M = majority(A, B, C). A second gate forms G = majority(A, B, not C), and the sum is S = majority(not M, G, C), where C has passed one buffer pair. The two inversions are reversed links.

State is a loop of four pairs, one per clock phase (Figure R2(b)). The loop carries a bit round once per period and so keeps it. A majority gate in the loop sets or clears it. The serial adder keeps its carry in such a loop, and the accumulator keeps a word of eight bits in a longer one. Both were run in the dual-rail form, in which the loop is closed across the two rails and no link is reversed (Table R9). A loop on one rail was not run in the batches of this Part.

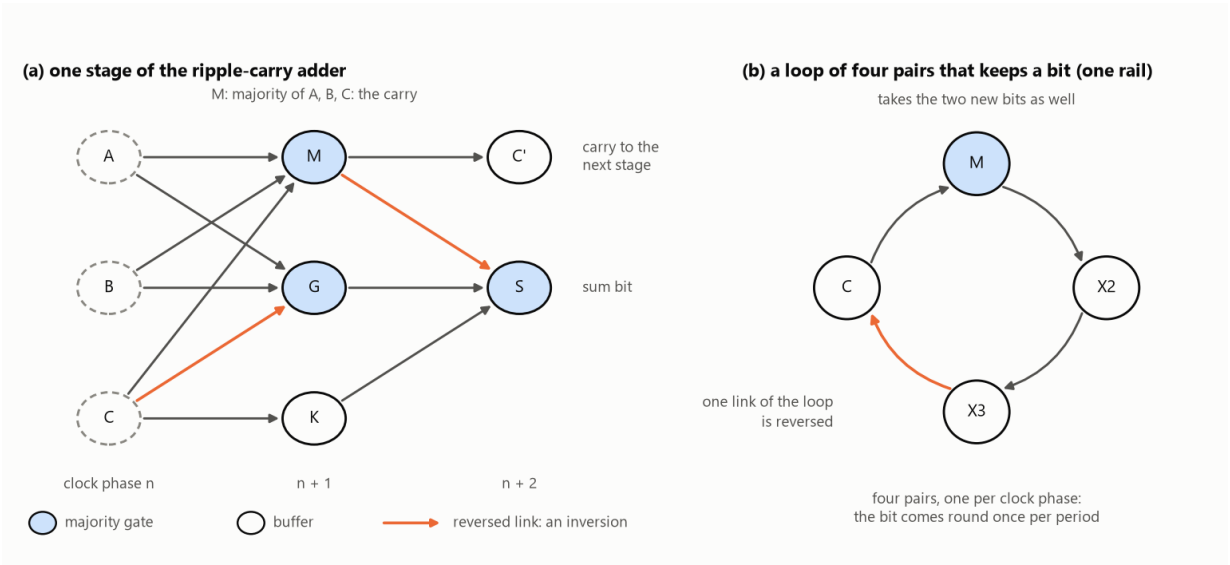


Figure R2. Logic and state (design). (a) One stage of the ripple-carry adder: five pairs, of which M, G and S are majority gates and K and C′ are buffers; the two orange links are reversed and act as inversions. (b) A loop of four pairs that keeps a bit, drawn on one rail with one link reversed. The serial adder and the accumulator that were run are dual-rail and close their loops across the two rails instead.

5.5 The model

The model is a time-domain circuit model of the pairs and their links. The pump, the clock, the inputs and the outputs are ideal sources. The equations below are those of one half of a pair, h = + or -, with the values of Table R3. The package of Appendix RA holds the model, and its file MODEL.md gives every equation and constant.

The circuit of one half. The clocked source reaches the supply node b through the source resistance R_b, and C_b loads that node. From node b the contact resistance ρ leads to the junction, which is the junction capacitance C_d in parallel with the diode's conduction current i_x. The junction ends on a pad p. The pad carries the tank capacitor C_p and one half winding of the inductor with its damping resistor R_L. A short stub of 0.637 fF and 6.37 pH behind 1 Ω stands for the lead at which a pair is driven and read.

$$C_p\, dv_p/dt = (v_b - v_j - v_p)/\rho - i_L + i_s \qquad \text{(R1)}$$

$$C_d\, dv_j/dt = (v_b - v_j - v_p)/\rho - i_x \qquad \text{(R2)}$$

$$C_b\, dv_b/dt = (v_{clk} - v_b)/R_b - \Sigma_h\, (v_b - v_{j,h} - v_{p,h})/\rho \qquad \text{(R3)}$$

$$L\, di_L/dt = v_p - R_L\, i_L \qquad \text{(R4)}$$

Here v_p is the pad voltage, v_j the voltage across the junction, v_b the voltage of the supply node, i_L the winding current and i_s the current from the stub. In (R4) the vector i_L holds the winding currents of all halves of a layout, and L is their inductance matrix. Inside a pair its two halves are coupled by k = 0.3: the inductance matrix of a pair is $[[L_h, -kL_h], [-kL_h, L_h]]$ with L_h = 20.23 pH, so that the antiphase mode sees $L_h(1 + k)$ = 26.3 pH per half. Between two linked pairs the antiphase modes share the mutual inductance

$$M = -0.06\, s\, (L_a\, L_b)^{1/2} \qquad \text{(R5)}$$

with L_a and L_b the antiphase inductances of the two pairs, s = +1 for a link that copies and s = −1 for a reversed link that inverts. A link that copies therefore has M = −1.58 pH in the 225-GHz design.

The diode. The static curve J(u) of the diode voltage u is a fitted law with a peak of 25.4 mA at 0.75 V and a valley of 11.4 mA at 1.30 V for the full published device; one diode of the cell carries a quarter of it. Appendix RA gives the law in full. The conduction current follows the curve with a first-order lag of the diode delay τ_d:

$$\tau_d\, di_x/dt = (1/4)\, J(v_j) - i_x \qquad \text{(R6)}$$

Clock, pump and input. For a pair at clock depth d, with w(t) the clock window of that depth,

$$v_{clk}(t) = V\, w(t)\, [1 + p\, \cos(4\pi f\, t + \theta_d)], \quad \theta_d = \pi\, (0.25 + 1.5\, d) \qquad \text{(R7)}$$

with V = 0.94 V, p = 0.25 and f the carrier frequency. During the first 14.3 ps of a run the supply is also multiplied by a linear start ramp (Appendix RA). An input pair is driven by a current of 0.4 mA at the carrier frequency into its two ends, in antiphase, with the sign of the data bit. The outputs are read; they are not loaded.

Noise. Every resistor carries its thermal noise at 353 K. The conduction current of every diode carries shot noise with a factor of 1, which is full shot noise. Both are assumptions; Section 9 says what a larger shot-noise factor would cost. The 225-GHz design and the 1-THz-class cell are one circuit in scaled units, and the noise power of the second, against the same signal, is 4.78 times that of the first.

Integration. The lumped equations are stepped with the trapezoidal rule, and the stub with a staggered scheme, at a time step of 11.9 fs for the 225-GHz design (2.5 fs for the 1-THz-class cell). The reported batches ran on a graphics processor, with the state in single precision. Two check batches ran in double precision on a processor. Appendix RA gives the checks of time step, grid and precision.

Reading. The signal of a pair is half the difference of its two end voltages. Its level and phase are fitted over windows of 4.78 ps (1 ps for the 1-THz-class cell). A decision is read in the first window that starts at least 4.78 ps after the next clock phase has come on, which is a quarter period after the middle of the pair's own rising edge. At that moment the pairs fed by this one take their decision. A decision is counted wrong when its phase lies more than a quarter turn from that of the same run without noise and without spread. That reference run is itself checked against the expected bits: a pair is right when, in every counted slot, its signal has the sign of the expected bit along the pair's own axis, which is fitted to that run. In rows this check reads the last window of the on-time, and in gates and in layouts with state it reads the decision window. The first slot of a run follows a clock cycle without data and is left out of every count, and so is a bit that the layout does not define.

Levels. The "lowest level" of a layout is the smallest level in the decision window over its pairs and counted slots, in the run without noise or spread. The comparison of codes reads another window, two carrier periods long, that starts 2 ps after the next clock phase has come on. That reading is named where it is used (Table R16, Table R29).

What the model leaves out. The pump source and its distribution, the clock network, the circuits for inputs, outputs and constants, every wire, the substrate, radiation and heat. Section 14 lists them.

6 One pair

Everything in this Part rests on what one pair does when it is pumped. This section shows it for one pair of the 225-GHz design on a constant supply, without clock and without neighbours. Section 6.5 also reads a row and a serial adder under the clock. Sections 6.1 and 6.3 to 6.5 are in-model, in this Part's code only. Section 6.2 quotes a linear analysis that is not a run, and Section 6.6 gives the other codes.

6.1 Silent without the pump, two phases with it

A small seed at the carrier frequency is applied for 28.7 ps with one of twelve starting phases and then removed. Table R4 gives the level of the oscillation that is left after 520 to 570 ps, and whether the twelve runs end on two phases.

Table R4. One pair on a constant supply: level per half of the 225-GHz oscillation after 520 to 570 ps, from twelve starting phases (in-model, in one code). “Two phases”: the twelve runs end within 10 degrees of two phases half a turn apart. The time is counted from the start of the 28.7-ps seed and read in windows of 4.8 ps; it is when the runs were within those 10 degrees for good. “Any phase”: the pair oscillates and keeps the phase it started with. The table is a selection: its source also has pumps of 20 and 30 % and supply levels of 0.82 and 0.85 V.

Pump	0.88 V	0.91 V	0.94 V	0.97 V	1.00 V	1.03 V	1.06 V
none	silent	silent	silent	160 mV, any phase	224 mV, any phase	258 mV, any phase	279 mV, any phase
10 %	silent	silent	143 mV, two phases, 38 ps	211 mV, two phases, 38 ps	247 mV, two phases, 67 ps	273 mV, two phases, 191 ps	291 mV, two phases, 263 ps
15 %	silent	silent	171 mV, two phases, 33 ps	219 mV, two phases, 33 ps	251 mV, two phases, 48 ps	275 mV, two phases, 105 ps	272 mV, any phase
25 %	58 mV, two phases, 33 ps	148 mV, two phases, 33 ps	193 mV, two phases, 29 ps	225 mV, two phases, 33 ps	248 mV, two phases, 38 ps	264 mV, two phases, 67 ps	229 mV, any phase
40 %	124 mV, two phases, 33 ps	146 mV, two phases, 33 ps	143 mV, two phases, 33 ps	silent	silent	silent	silent

- **Without a pump the pair is silent below 0.97 V.** From 0.97 V it oscillates by itself and keeps whatever phase it started with.
- **With the pump it oscillates below 0.97 V as well:** down to 0.94 V with a 10 % pump and to 0.88 V with 25 %. There it has exactly two phases. The twelve runs are within 10 degrees of them for good 29 to 38 ps after the seed is applied. The seed itself lasts 28.7 ps, so the pair is on its two phases at most about 10 ps after the seed is removed.
- **Above its own threshold the pump only steers, and not everywhere.** The pair already oscillates, and the pump has to turn its phase. With a 10 % pump that takes 67 ps at 1.00 V, 191 ps at 1.03 V and 263 ps at 1.06 V. At 1.06 V pumps of 15 and 25 % do not set the phase: the pair keeps the phase it started with. A pump of 40 % silences the pair from 0.97 V, and in the finer scan of Figure R3 a pump of 35 % silences it from 1.02 to 1.13 V. In that scan, in steps of 10 mV up to 1.16 V, the pair loses its two phases only in a band: at 1.06 V with a 25 % pump, and from 1.06 to 1.08 V with 15 %. Above the band it is on two phases again up to the end of the scan, and so it is from 1.14 V with 35 %. The cause of the band was not examined. This is the regime of the phase logic with self-sustaining oscillators of Section 3. The design does not use it.
- **So the operating point lies just below the threshold:** 0.94 V with a 25 % pump (design). The level there is 193 mV per half, and six of the twelve starts end on each phase.

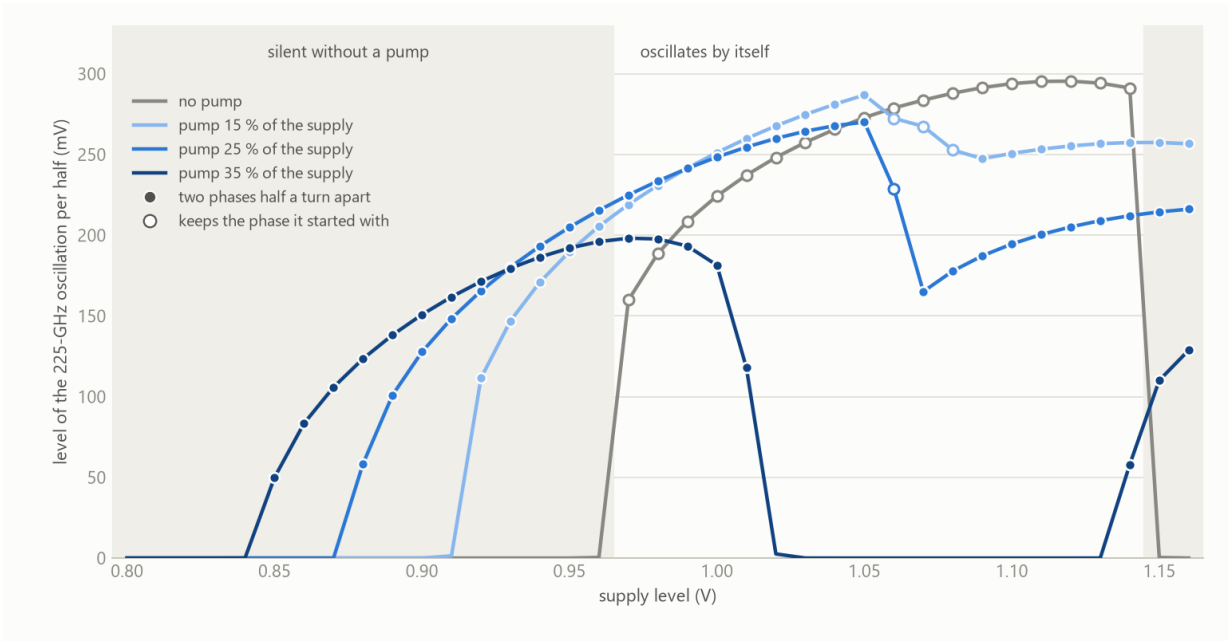


Figure R3. One pair on a constant supply: level per half of the 225-GHz oscillation against the supply level, without a pump and with pumps of 15, 25 and 35 % of the supply level, from a finer scan than Table R4 (in-model, in one code). Filled points: the

twelve starting phases end on two phases half a turn apart. Open points: the pair keeps the phase it started with. In the grey bands the pair is silent without a pump.

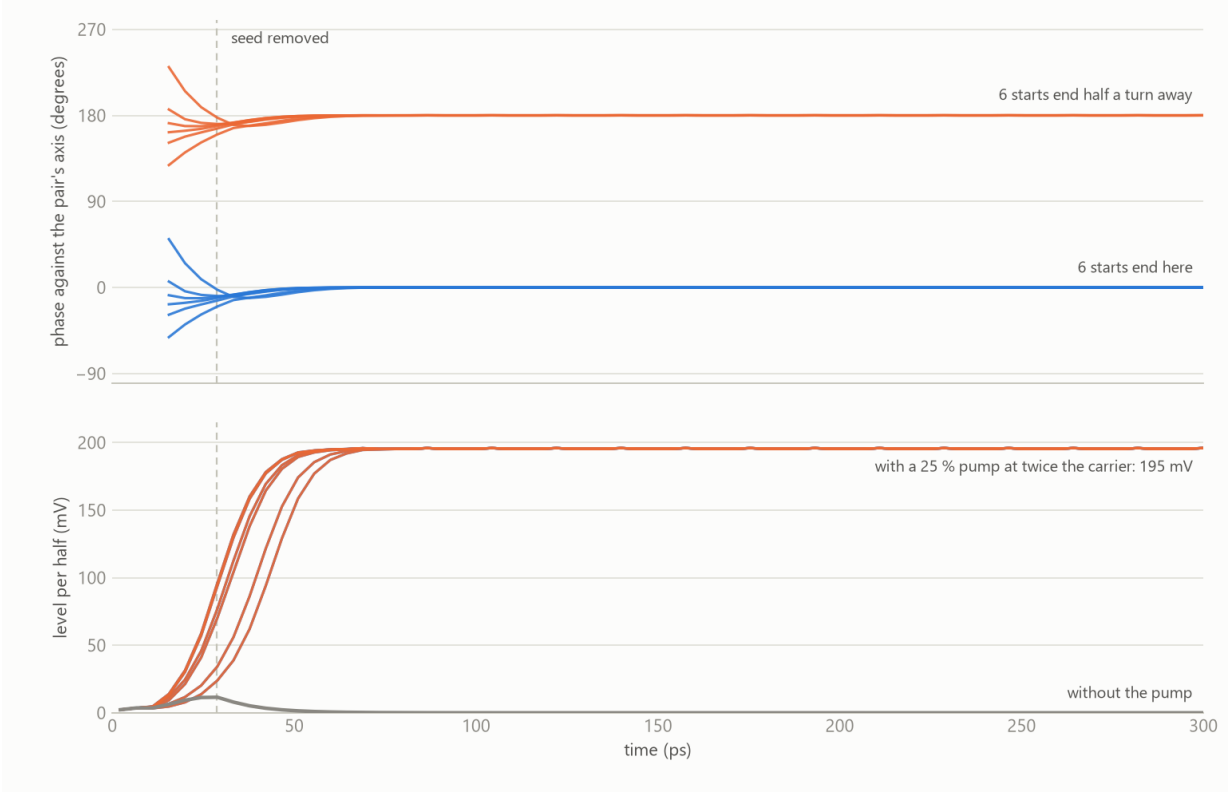


Figure R4. One pair at 0.94 V from twelve starting phases (in-model, in one code). Top: phase against the pair's axis. Bottom: level per half, read per whole carrier period. With a 25 % pump at twice the carrier six starts end on one phase and six half a turn away, and the level settles at 195 mV when read per whole carrier period; the windows of Table R4 give 193 mV. Without the pump the level decays to zero. The seed is removed at the dashed line.

6.2 Why the pump does this

Below its threshold the conductance of the diodes is too weak to carry an oscillation. The pump swings the supply by a quarter of its level. For part of every pump cycle that carries the diodes into the steep part of their curve, and it does so in step with one of the two quadratures of the carrier. That quadrature grows and the other decays. A reader's linear analysis of this cell gives both rates at 0.95 V with a 20 % pump: +0.14 per ps for the one and -0.23 per ps for the other. That is an analysis, not a run of the model, and this account of the mechanism is an interpretation.

The two phases that result are fixed by the phase of the pump. The line through them is called the pair's axis. A weak input along that axis decides which of the two the pair takes, and the pair then restores the full level. That is the restoring step of the logic.

6.3 What the pump source carries

At 0.94 V with a 25 % pump the pump term of the supply source is 235 mV, and the source passes 6.1 mA at 450 GHz. The current is almost all reactive. On balance the pair returns 0.006 mW to the pump source there, and at 0.88 V it absorbs 0.05 mW. The pair draws 10.5 mA of direct current (in-model, in one code). Section 2.4 uses these values for the pump power per pair.

6.4 What one pair stands in its inductance

With a 25 % pump at 0.94 V an isolated pair stays on two phases when its inductance is off by 15 % downward to 30 % upward, the end of the scan. At 15 % downward its level is 47 mV, against 193 mV without error. Its axis turns by 0.7 to 1.0 degree per per cent of a downward error and by 1.2 to 1.6 degrees per per cent of an upward one, which is 48 degrees at 30 % upward. At 20 % downward it is silent (in-model, in one code).

How large an error of its own inductance a single pair inside a fabric of pairs stands was not counted in the runs of this Part. Section 7.3 gives the spread that a row of sixteen stands: it holds at 6 % rms and not at 8 %.

6.5 The in-phase mode

The two ends of a pair can also swing in phase. A reader's linear analysis found that mode unstable from 1.00 to 1.065 V, near 282 GHz. The runs of this Part read only the antiphase signal and would not show it, so it was tested directly.

Table R5. The in-phase mode (in-model, in one code). The in-phase voltage is half the sum of the two end voltages. For the single pair, "what is left" is that voltage 146 to 170 ps after a small in-phase kick, with a constant, a slope and, where there is a pump, the parts at the pump frequency and its second harmonic removed. Under the clock it is that voltage on the flat top of the on-time, with a constant, a slope and the first four harmonics of the carrier removed, as the median over pairs and slots.

Test	Result
One pair, nothing else oscillating, no pump	an in-phase oscillation at 281 GHz grows from 1.00 to 1.06 V, and 32 to 60 mV of it is left from 1.01 to 1.06 V; it decays below 1.00 V and from 1.07 V
The same with a 5 % pump	grows from 1.01 to 1.06 V
The same with a 10 % pump	decays at every level, slowly from 1.02 to 1.05 V, where 9.4 to 23.7 mV is left
The same with a pump of 15 to 30 %	decays at every supply level from 0.94 to 1.10 V; at most 1.4 mV is left
Row of eight under the clock, 25 % pump, 0.88 to 1.03 V, without noise or spread	second half of the flat top: 0.7 to 1.5 mV (largest 2.6 mV); first half: 3.1 to 13.0 mV, rising with the supply level; the signal is 85 to 287 mV
The same row with the noise of the 225-GHz design and a 3 % spread of the inductance, two runs per level	second half: 6.4 to 7.1 mV (largest 13.2 mV), the same at every supply level; first half: 7.4 to 15.1 mV
Serial adder under the clock, 25 % pump, at 0.94, 1.00 and 1.015 V, without noise or spread	second half: 1.2 to 1.3 mV (largest 6.8 mV); first half: 6.3 to 12.0 mV
The same adder with that noise and a 3 % spread, two runs per level	second half: 6.8 to 7.2 mV (largest 14.7 mV)

The instability is real in the model. With a pump of 15 to 30 % the mode decays at every supply level from 0.94 to 1.10 V, and at most 1.4 mV of it is left after 146 to 170 ps. At the 25 % of the design it decays slowly, by 0.0004 to 0.0030 per ps, from a small start. Pumps above 30 % were not tested in this way.

Under the clock, what is left in phase in the second half of the flat top is a few millivolts with noise and does not grow with the supply level. In the first half it does grow: in the row of eight its median rises from 3.1 mV at 0.88 V to 13.0 mV at 1.03 V without noise. The upper ends of the working ranges in Sections 7 and 8 are therefore not set by this mode, as far as it was tested under the clock. That is with a 25 % pump, up to 1.03 V in a row and up to 1.015 V in the serial adder. A design with a weak pump would have to stay below 1.00 V.

6.6 What other codes find for one pair

Three other codes of the same circuit were written from specifications alone (Appendix RA). In the second, the pair oscillates by itself from 0.97 to 1.14 V, at 224.3 GHz at 1.05 V. This Part's model gives the same range, and 224.7 GHz at 1.06 V. The third and the fourth also find 0.97 to 1.14 V. With a 25 % pump at 0.94 V those two find the oscillation at exactly half the pump frequency, on two phases half a turn apart, with six of twelve starts on each. The second code ran a pump on a constant supply only for another candidate cell (in-model: the range in three codes besides this Part's, the pumped result in two).

7 Rows

A row is the simplest fabric of pairs: every pair copies the pair before it, one clock phase later. It tests transport and restoration without logic. All results of this section are in-model, for the 225-GHz design with links of 6 % and a slot of 69 ps unless a line says otherwise, at the noise of that design. Full shot noise is an assumption of the model, and every statement below on raised noise rests on it. Apart from the lines named in Section 7.4, the results were run by this Part's model only.

7.1 Where a row of sixteen holds

A row of sixteen pairs is fed a pattern of bits at its first pair. Each point is run 32 times with noise and with a 3 % spread of the inductance from pair to pair, and once without either. Seven slots are counted per run, so each point has 224 decisions at any one pair.

A row is said to **hold** at a point when three things are true. Pairs 1 to 15 are right in the run without noise or spread; at every point that holds, all sixteen are. No decision of pair 14, the last pair but one, is wrong in the 32 runs. And the phase of that pair differs from its noiseless phase by at most 8 degrees root-mean-square (rms). The third condition is a margin, not an error: a row can miss it without a single wrong decision.

Table R6. Supply levels at which a row of sixteen holds, with a 3 % spread of the inductance and the noise of the 225-GHz design (in-model; 32 runs per level; scanned from 0.850 to 1.105 V in steps of 15 mV). Every range is unbroken. The lines at 15, 25 and 35 % were also run by a second code (Section 7.4), the others by one code.

Pump level	Holds at	Supply levels
15 %	0.925 to 0.970 V	4
20 %	0.895 to 1.000 V	8
25 %	0.880 to 1.030 V	11
30 %	0.865 to 1.045 V	13
35 %	0.850 to 1.030 V	13
40 %	0.850 to 0.985 V	10

Note: at 0.985 V with a 40 % pump one decision of the last pair, pair 15, is wrong in one of the 32 runs. The rule does not check that pair.

At the 25 % pump of the design the row holds at all eleven levels run from 0.880 to 1.030 V. The lower end of the ranges at 35 and 40 % is the end of the scan. The ranges reach above 0.97 V, the level from which a pair oscillates by itself, because a pump of 20 % or more still sets the phase there (Section 6). Half the time step changes no decision of a row of sixteen at 0.880, 0.94 and 1.015 V, and changes levels by at most 2.4 %. That check was made without noise, and with noise at 0.94 V only (Appendix RA).

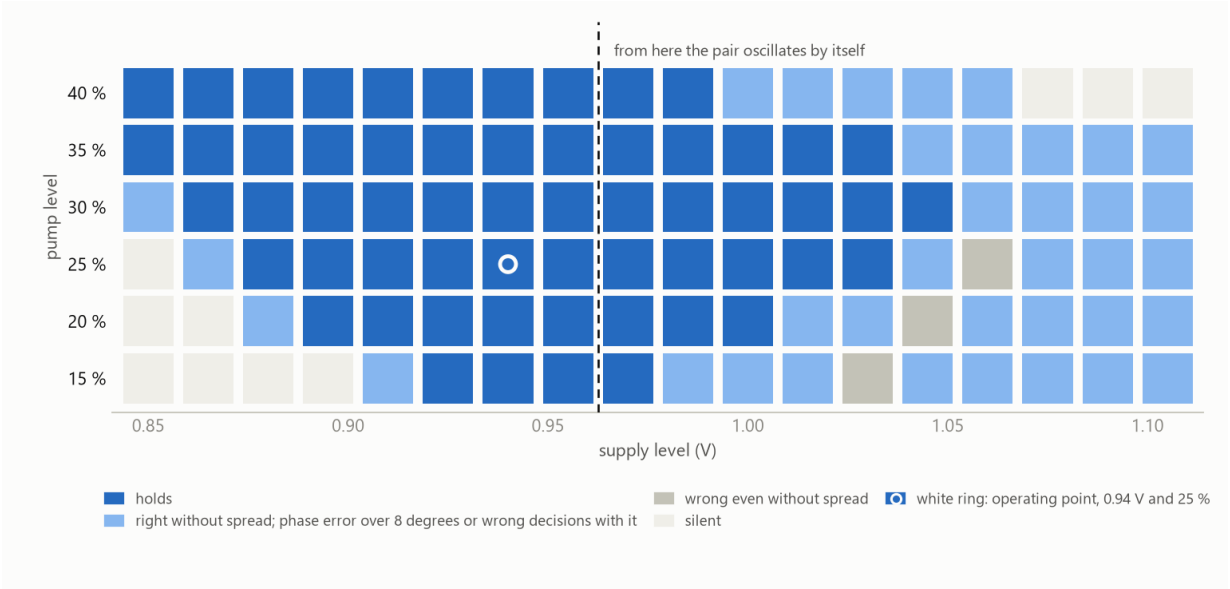


Figure R5. Where a row of sixteen holds, in the plane of supply level and pump level (in-model; a 3 % spread of the inductance and the noise of the 225-GHz design; each box is 32 runs). Dark: the row holds. Light: every pair is right without noise or spread, but with them the phase error at pair 14 exceeds 8 degrees or a decision of pair 14 is wrong. Grey: wrong even without spread, or silent. The ring marks the operating point; the dashed line is the level from which a pair oscillates by itself.

7.2 Rows of 92

Part III's critical path is 92 cells long (Part III, Section 4.3; in-model there). That length is used here as a row length and as nothing else.

Table R7. Rows of 92 pairs at 0.94 V with a 25 % pump (in-model, in one code; 32 runs of 7 counted slots per line; the noise of the 225-GHz design in every line). A first-wrong event is the first wrong decision along the row in one slot of one run. The decisions at risk are those of the pairs after the input pair, up to that event, or of the whole row where there is none.

Condition	Pairs right without noise or spread	First-wrong events in decisions at risk	rms phase error at pairs 10 / 30 / 60 / 90
No spread	92 of 92	0 in 20,384	0 / 0 / 0 / 0 degrees
Inductance spread 3 %	92 of 92	0 in 20,384	3 / 4 / 3 / 3 degrees
Inductance spread 5 %	92 of 92	0 in 20,384	5 / 4 / 5 / 5 degrees
Seven spreads at once, pump phase 20 degrees	92 of 92	0 in 20,384	10 / 10 / 9 / 8 degrees
No pump	5 of 92	224 in 1,160	99 / 108 / 105 / 101 degrees

"Seven spreads at once" are these, all rms from pair to pair. Three are spreads of the parts: an inductance spread of 3 %, a diode current spread of 5 % and a difference inside a pair of 2 %. Four are errors of what a pair is fed: a pump level error of 10 %, a link strength error of 10 %, a clock timing error of 2 % of the period, and a pump phase error. The pump phase error is named each time the set is used. It is 20 degrees in this section and 10 degrees in the full set of Section 8.5. It is counted in degrees of the pump wave, which is half as much in carrier phase.

- **A row of 92 carries its data without a first wrong decision in 20,384 decisions at risk,** under each of the four conditions with the pump (a count, not a rate).
- **The phase error does not grow along the row.** It is no larger at pair 90 than at pair 10. Every pair restores the phase as well as the level.
- **Without the pump the row carries nothing.** In the run without noise or spread its level falls to zero by pair 5. Of the five pairs that are right, four are pairs 0 to 3, next to the input, and one is pair 63.
- **What the zero bounds.** If the 20,384 decisions were independent, a count of zero would bound the rate of wrong decisions from noise to at most 1.8×10^{-4} per decision, the upper end of the exact 95 % interval (this paper's arithmetic). The 32 draws of the spreads bound the share of rows that fail only to at most 10.9 %. Neither is close to the pass line of 6.3×10^{-9} per cell decision that Part III derives for its lane (Part III, Section 5.2; in-model there, an upper bound), and no rate is claimed.
- **With seven spreads and a pump phase error of 20 degrees the phase error is 10 degrees at the first pairs.** That exceeds the 8 degrees of the holding rule, so this line is reported as "no first wrong decision" and not as "holds".

7.3 What a row tolerates

One quantity is varied at a time, on a row of sixteen at the operating point. Every line carries a 3 % spread of the inductance and the noise of the 225-GHz design unless it says otherwise.

Table R8. Single tolerances of a row of sixteen at 0.94 V with a 25 % pump (in-model, in one code; 32 runs of 7 counted slots per value). "No wrong decision" means none at pair 14 and no first-wrong event anywhere in the row. Pump phase errors are in degrees of the pump wave, which is half as much in carrier phase.

Quantity varied (rms from pair to pair unless stated)	Holds at	Does not hold at
Supply level	1, 2, 3, 4 and 5 % (5 % is 47 mV)	none of the values run
Damping resistor	5, 10, 20 and 30 %	none of the values run
Pump phase, from pair to pair	10 degrees	20 and 30 degrees, by the phase-error rule alone (11.2 and 14.9 degrees, no wrong decision); 45 degrees with 25 wrong decisions of 224; 60 degrees with 61 of 224
Pump phase, of a whole clock phase	5 and 10 degrees	20 and 30 degrees, by the phase-error rule alone (8.6 and 11.0 degrees); 45 degrees with 6 wrong of 224
Pump level	20 and 30 %	none of the values run
Link strength, all links alike (the design has 6 %)	2, 3, 4.5, 7.5, 9 and 12 %	none of the values run
Link strength, from link to link	10, 20 and 30 %	none of the values run
Inductance	3, 5 and 6 %	8 and 10 %, by the phase-error rule alone (9.1 and 13.0 degrees, no wrong decision)
Diode current; difference inside a pair	10 %; 5 %	not run further

Quantity varied (rms from pair to pair unless stated)	Holds at	Does not hold at
Clock timing	2 and 5 % of the period (5 % is 3.5 ps)	10 % (7 wrong of 224)
Slot, with the on-time at 0.75 of it	38, 48, 57, 81 and 96 ps	none of the values run
On-time at the slot of 69 ps	0.50 and 0.60 of the slot	none of the values run
Carrier and pump against the tanks	2 and 3 % up or down in frequency	none of the values run
Seven spreads at once, pump phase 20 degrees		does not hold by the phase-error rule alone (10.0 degrees; no wrong decision)
The full set of nine spreads (pump phase 10 degrees; Section 8.5), and the same with twice the supply level error and resistor spread	both hold (5.5 and 6.2 degrees)	
Noise power, without spread, 127 runs	1, 4.78, 16, 64 and 128 times that of the 225-GHz design	256 times (63 wrong of 889); about 1,020 times (408 of 889)

Note: the line on noise power assumes full shot noise, as every run does. A margin in noise power is a margin against that assumption.

- **A row holds at every value run of most quantities,** one at a time. They are a supply level error up to 5 % rms, a damping resistor spread up to 30 %, a pump level error of 20 and 30 %, and a link strength from 2 to 12 %, which is a third to twice the design's. They are also a link strength error up to 30 % from link to link, the diode spreads that were run, slots from 38 to 96 ps, on-times of 0.50 and 0.60 of the slot, and a carrier 2 and 3 % off the tanks. Where these edges lie was not found. These are counts in 32 runs of 7 slots, not rates.
- **It does not hold** with an inductance spread of 8 %, with a clock timing error of 10 % of the period, or with seven spreads at once and a pump phase error of 20 degrees. The first and the third fail by the phase-error rule alone, without a wrong decision.
- **The pump phase is the tightest tolerance of a row.** It holds at 10 degrees of the pump wave and not at 20, from pair to pair or for a whole clock phase, and nothing between was run. Beyond 10 degrees the phase error grows past the margin of the holding rule before any decision is wrong. The full set of spreads carries 10 degrees.
- **The input must stay out of one band of phase.** The input phase was stepped over a full turn of pump phase in sixteen steps. The row holds at 14 of them. It fails at the two that lie 0.875π and 1.0π above the aligned value, where the first pair already errs: 25 and 13 wrong of 224 at pair 0, and 31 and 13 at pair 14. At 64 times the noise power, without spread and with 64 runs per phase, it holds at 12 of the sixteen. The aligned value of the design lies opposite that band.

7.4 What a second code finds for rows

A second code (Appendix RA) ran rows of sixteen of the design at the noise of the 225-GHz design, with a 3 % spread of the inductance, 8 draws of 10 counted slots per point and the same rule for holding. It holds from 0.925 to 0.985 V at a 15 % pump, from 0.880 to 1.030 V at 25 % and from 0.850 to 1.030 V at 35 %, where 0.850 V is the bottom of its scan. This Part's model, with 32 draws of 7 slots, gives 0.925 to 0.970 V, 0.880 to 1.030 V and 0.850 to 1.030 V (Table R6). The ranges are the same at 25 %, and so are the upper ends at 35 %. At 15 % the upper ends differ by one step of 15 mV. There this Part's model fails at 0.985 V by the phase-error rule alone, with 8.6 degrees and no wrong decision (in-model, two codes). Section 11.4 gives the comparison of the codes at the noise of the 1-THz-class cell.

8 Logic and state

This section holds the main result of the Part and its edge. Adders and layouts with state compute in the model with noise and with single spreads of the sizes named below. With all nine spreads at once, whose pump phase error is 10 degrees, the four-bit adder fails in 5 and in 7 of 256 draws at the noise of the 225-GHz design and of the 1-THz-class cell (counts, not rates). All results are in-model, for the 225-GHz design at 0.94 V with a 25 % pump, links of 6 % and a slot of 69 ps unless a line says otherwise, at the noise of that design, with full shot noise assumed. Apart from the lines of the serial adder named in Section 8.7, they were run by this Part's model only. Section 11 repeats the adders at the noise of the 1-THz-class cell.

8.1 The layouts

Five layouts were run (Table R9). In the ripple-carry adders every stage has the five pairs of Figure R2(a), and the operands reach each stage through rows of buffer pairs, so that all inputs of a gate arrive in the same clock phase. An adder takes a new pair of operands in every slot and delivers each sum a fixed number of slots later: it is wave-pipelined. The serial adder takes one bit of each operand per slot and keeps its carry in a loop of four pairs. The accumulator adds a number to a stored word of eight bits, bit by bit.

Table R9. The layouts (design).

Layout	Pairs	Links	Reversed links	What a run is
Four-bit ripple-carry adder	53	68	8	31 additions of pseudo-random operands, one per slot
Eight-bit ripple-carry adder	169	200	16	the same
Four-bit adder on two rails	106	136	none	the same
Serial adder with a stored carry, two rails	20	28	none; the carry loop is closed across the rails	one addition of two 31-bit numbers, one bit per slot
Eight-bit accumulator, two rails	84	96	none; its loops are closed across the rails	four words of eight sum bits

Unless stated, a line has 32 runs: 32 draws of the spreads, each with its own noise. For the four-bit adder that is 992 additions and 52,576 decisions of single pairs. An addition is wrong when any output bit is wrong. A sum of the serial adder is wrong when any of its 31 bits is wrong. A line is called **clean** when every pair is right in the run without noise or spread, no result is wrong and no pair takes a wrong decision in any run.

Part III prices a threshold full adder of five cells, whose carry is a majority, for a cell that thresholds a three-way sum, and labels it open (Part III, Section 8.1(a)). It leaves a dual-rail lane uncounted (Part III, Sections 4.2 and 9). The counts of Table R9 are counts in another device and are not set against Part III's.

8.2 The adders

Table R10. The four-bit adder (in-model, in one code; 32 runs per line; every line with noise and a 3 % spread of the inductance, except the first, which has no spread, and the line at 5 %).

Condition	Wrong additions of 992	Runs with a wrong addition, of 32	Lowest level without noise
Operating point, no spread	0	0	201 mV
Operating point, inductance spread 3 %	0	0	201 mV
Operating point, inductance spread 5 %	0	0	201 mV
Supply 0.880 V	316	30	2 mV
Supply 0.895, 0.910, 0.970, 0.985, 1.000 and 1.015 V	0 at each	0	87 to 245 mV
Pump 15, 20, 30 and 35 %	0 at each	0	
Pump 40 %	8	3	77 mV
Links 3, 4.5, 7.5 and 9 %	0 at each	0	
Links 12 %	wrong without noise: 41 of 53 pairs right		
Slot 38 ps	1	1	34 mV
Slots 48, 57 and 81 ps	0 at each	0	

- **At the operating point the four-bit adder is clean,** with no spread and with an inductance spread of 3 % or 5 %: no wrong decision among 52,576 in each line (a count, not a rate).
- **It is clean at the six levels run from 0.895 to 1.015 V,** the upper end of the scan, and at the operating point of 0.940 V. Other levels between them were not run. At 0.880 V it fails in 30 of 32 runs.
- **It is clean at the pumps run from 15 to 35 %, at the links run from 3 to 9 % and at slots of 48, 57 and 81 ps.** A pump of 40 % gives 8 wrong additions in 3 runs, and a slot of 38 ps one wrong addition. Links of 12 % give wrong pairs even without noise.

Table R11. The eight-bit adder of 169 pairs and the four-bit adder on two rails, of 106 pairs (in-model, in one code; 32 runs per line; 992 additions per line; 167,648 decisions of single pairs in the eight-bit adder and 105,152 in the adder on two rails).

Layout and condition	Wrong additions of 992	Runs with a wrong addition, of 32	Lowest level without noise
Eight-bit adder, operating point, no spread	0	0	197 mV
Eight-bit adder, inductance spread 3 %	0	0	197 mV
Eight-bit adder, inductance spread 5 %	0	0	197 mV
Eight-bit adder, seven spreads at once, pump phase 20 degrees	7	1	197 mV
Eight-bit adder, half of the full set of nine (pump phase 5 degrees), two samples	0 in each	0	197 mV
Eight-bit adder, supply 0.910 and 0.970 V, inductance spread 3 %	0 at each	0	
Adder on two rails, operating point: no spread; inductance spread 3 %; 5 %	0 at each	0	201 mV
Adder on two rails, seven spreads at once, pump phase 20 degrees	12	1	201 mV

- **The eight-bit adder is clean at the operating point,** with no spread and with an inductance spread of 3 % or 5 %: no wrong decision among 167,648 in each line (a count, not a rate). Its lowest level is 197 mV, against 201 mV in the four-bit adder: the longer carry chain costs 4 mV.
- **With seven spreads at once and a pump phase error of 20 degrees it has 7 wrong additions, all in one run of 32.** The four-bit adder has 4 in one run with that set (Section 8.5). With seven spreads and 10 degrees the eight-bit adder was not run. With half of the full set of nine, whose pump phase error is 5 degrees, it is clean.
- **The full set of nine spreads (pump phase error 10 degrees) was not run on the eight-bit adder.** The spread budget of Section 8.5 is that of the four-bit adder.
- **The four-bit adder on two rails is clean at the operating point as well,** with no reversed link: no wrong decision among 105,152 in each line, with no spread and with an inductance spread of 3 % or 5 %. With seven spreads at once and a pump phase error of 20 degrees it has 12 wrong additions, all in one run of 32.

8.3 State

The serial adder holds its carry in a loop of four pairs. In the run of 31 slots it keeps a stored 1 through eight slots in a row, and a stored 0 through nine, in which the two operand bits differ, so that only the loop holds the carry.

Table R12. The serial adder with a stored carry (in-model; 32 runs per line; every line with noise and a 3 % spread of the inductance, except the first, which has no spread, and the line at 5 %). A second code also ran the lines on supply level, pump level and link strength (Section 8.7).

Condition	Wrong sums of 32	Runs with a wrong decision of any pair, of 32	Lowest level without noise
Operating point, no spread	0	0	204 mV
Operating point, inductance spread 3 % or 5 %	0	0	204 mV
Supply 0.880 V	18	23	29 mV
Supply 0.895, 0.910, 0.970, 0.985, 1.000 and 1.015 V	0 at each	0	
Pump 15, 20, 30, 35 and 40 %	0 at each	0	
Links 3, 4.5, 7.5 and 9 %	0 at each	0	
Links 12 %	wrong without noise: 16 of 20 pairs right		
Slots 38, 48, 57 and 81 ps	0 at each	0	83 mV at 38 ps

- **The stored carry is kept without a wrong decision** among 19,840 in each line at the operating point (a count, not a rate).
- **The serial adder has the working ranges of the four-bit adder,** and is clean at a 40 % pump and at a slot of 38 ps as well.

The accumulator adds a number to a stored word of eight bits, one bit per slot, and feeds the sum back through a long loop of buffer pairs. A run has four words of eight sum bits.

Table R13. The accumulator of 84 pairs (in-model, in one code; 32 runs per line; 128 words and 82,880 decisions per line). The 82,880 leave out the decisions whose expected bit the layout does not define. Lines marked † carry a 3 % spread of the inductance on top.

Condition	Wrong words of 128	Runs with a wrong decision, of 32
Operating point: no spread; inductance spread 3 %; 5 %	0 at each	0
Supply 0.910 and 0.970 V †; pump 20 and 30 % †	0 at each	0
Pump phase error from pair to pair, 20 degrees	0	0
Pump phase error of a whole clock phase, 10 degrees †	0	0
Clock timing error, 5 % of the period	0	0
Supply level error, 2 % †	0	0
Damping resistor spread, 10 % †	0	0
Link strength error, 20 %	50	17
Seven spreads at once, pump phase 10 degrees	0	0
Seven spreads at once, pump phase 20 degrees	3	1
The full set of nine spreads (pump phase 10 degrees)	4	2
Half of the full set (pump phase 5 degrees)	0	0

- **The accumulator keeps its word and adds to it without a wrong decision** among 82,880 in each line at the operating point (a count, not a rate). Its lowest level without noise is 188 mV.
- **It stands the single tolerances at the values at which the adders are clean,** as far as they were run on it. A link strength error of 20 % fails here as it does in the adders, and more often: 17 of 32 runs. An error of 10 % was not run on this layout.
- **With the full set of nine spreads, whose pump phase error is 10 degrees, it has 4 wrong words of 128, and wrong decisions in 2 of 32 runs.** With half of the set it has none.
- **In a layout with state an error stays.** The two failing runs of the full set hold 549 wrong decisions (in-model). A wrong stored bit is carried round its loop until it is overwritten, while in an adder without state a wrong decision spoils one addition (design).

8.4 Single tolerances

One spread is applied at a time (Table R14). The lines of the second half of the table also carry a 3 % spread of the inductance; those of the first half do not.

Table R14. Single tolerances of the four-bit and the serial adder at the operating point (in-model, in one code; 32 runs per value; rms values from pair to pair). Each entry gives the values that were clean and the first value that was not, with its wrong additions of 992 or wrong sums of 32. In brackets are the runs with a wrong addition for the four-bit adder, which in these lines are also its runs with a wrong decision, and the runs with a wrong decision of any pair for the serial adder.

Quantity varied	Four-bit adder	Serial adder	Inductance spread on top
Pump phase, from pair to pair	clean at 10 and 20 degrees; 30 degrees: 45 (4)	clean at 10 and 20 degrees; 30 degrees: 2 (2)	none
Link strength, from link to link	clean at 10 %; 20 %: 101 (13)	clean at 10 %; 20 %: 2 (5)	none
Clock timing	clean at 2 and 5 % of the period	clean at 2 and 5 %	none
Pump level	clean at 20 %	clean at 20 %	none
Diode current; difference inside a pair	clean at 10 %; at 5 %	clean at 10 %; at 5 %	none
Stray inductive coupling between neighbours without a link	clean at 0.3, 0.6 and 1.2 %; on two rails clean at 0.3 and 0.6 %, and at 1.2 % wrong without noise (96 of 106 pairs right)	not run	none
Supply level	clean at 1, 1.5 and 2 %; 3 %: 34 (3)	clean at 1 and 2 %; 3 %: no wrong sum, one run with a wrong decision	3 %
Damping resistor	clean at 5 and 10 %; 15 %: 64 (7); 20 %: 172 (17)	clean at 5 and 10 %; 20 %: 2 (6); 15 % not run	3 %
Pump phase, of a whole clock phase	clean at 5, 10 and 20 degrees	clean at 5, 10 and 20 degrees	3 %
Input phase against the aligned value, in pump phase	clean at 0.125π and 0.25π either way	the same	3 %

- **The supply level from pair to pair binds.** The four-bit adder stands 2 % rms, which is 19 mV (this paper's arithmetic), and fails at 3 %. The serial adder is no longer clean at 3 %: it has no wrong sum, and one run with a wrong decision. A row alone holds at 5 % (Section 7.3).
- **The damping resistor comes next.** Both adders are clean at 10 %. The four-bit adder fails at 15 % and the serial adder at 20 %; 15 % was not run on it.
- **Both adders are clean with a pump phase error of 20 degrees** of the pump wave, from pair to pair or for a whole clock phase, and with a link strength error of 10 %. From pair to pair they fail at 30 degrees, and with a link strength error of 20 %.
- **Clock timing of 5 % of the period, a pump level error of 20 % and diode spreads of 5 to 10 % cost nothing** in these runs.
- **A stray inductive coupling between neighbours costs nothing up to 1.2 % on one rail and up to 0.6 % on two rails.** For this test the pairs are placed on a grid of clock phase against order, and every two neighbours on that grid that share no link are coupled, with alternating sign. The adder on one rail is clean at 0.3, 0.6 and 1.2 % of the pair's inductance, with its lowest level falling from 201 to 168 mV. The adder on two rails is clean at 0.3 and 0.6 % and has wrong pairs at 1.2 % even without noise; nothing between was run (32 runs per value, without other spread). The placement is an assumption: no layout was drawn.

8.5 All spreads at once: a spread budget

Spreads that are harmless one at a time cost something together. With the seven spreads of Section 7.2 at once and a pump phase error of 20 degrees, the four-bit adder has 4 wrong additions of 992, all in one run of 32, and the serial adder has none. With a pump phase error of 10 degrees instead, both are clean.

The full set of nine spreads takes those seven with the pump phase at 10 degrees and adds a supply level error of 1 % and a damping resistor spread of 5 %. With 32 draws the four-bit adder has wrong additions in 3 of 32 runs with the full set, and in none of 32 at three quarters, one half and one quarter of every value. The serial adder is clean with the full set and at three quarters and one half of it. That is a count in 32 draws, which bounds the failing share only below 11 %.

Thirty-two draws cannot size a failing share of a few per cent. The four-bit adder was therefore run with 256 draws per line, at fractions of the full set from one half upward and at both noise levels (Table R15, Figure R6). A draw is one set of values of all nine spreads for the 53 pairs. It fails if any of its 31 additions is wrong.

Table R15. The spread budget of the four-bit adder (in-model, in one code; 256 draws per line). The first column is the fraction by which every rms value of the full set is multiplied. The full set has a pump phase error of 10 degrees, so a fraction of one half has 5 degrees. The intervals are exact binomial 95 % intervals.

Fraction of the full set	Noise	Failing draws of 256	Share, with its 95 % interval	Wrong additions of 7,936
0.5	of the 225-GHz design	0	0 % (0 to 1.4 %)	0
0.75	of the 225-GHz design	0	0 % (0 to 1.4 %)	0
1	of the 225-GHz design	5	2.0 % (0.6 to 4.5 %)	26
0.5	of the 1-THz-class cell	0	0 % (0 to 1.4 %)	0
0.625	of the 1-THz-class cell	0	0 % (0 to 1.4 %)	0
0.75	of the 1-THz-class cell	1	0.4 % (0.01 to 2.2 %)	3
0.875	of the 1-THz-class cell	10	3.9 % (1.9 to 7.1 %)	24
1	of the 1-THz-class cell	7	2.7 % (1.1 to 5.6 %)	23

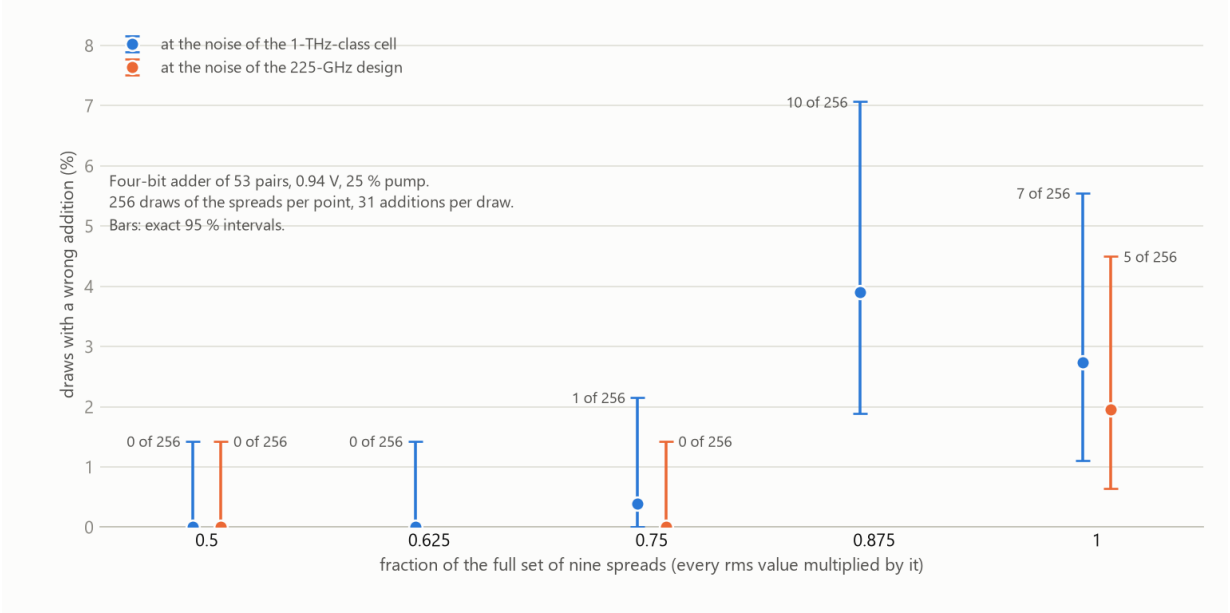


Figure R6. The spread budget of the four-bit adder: share of the draws of the nine spreads in which an addition is wrong, against the fraction of the full set, whose pump phase error is 10 degrees at the whole set, at the noise of the 225-GHz design and of the 1-THz-class cell (in-model, in one code; 256 draws per point; bars are exact 95 % intervals).

- **With the full set the adder fails in 2.0 % of the draws at the noise of the 225-GHz design and in 2.7 % at the noise of the 1-THz-class cell,** with intervals of 0.6 to 4.5 % and 1.1 to 5.6 %. A two-sided exact test finds no difference between the two noise levels (P = 0.77; this paper's arithmetic).
- **Two samples of that line differ.** At the noise of the 225-GHz design the full set failed in 3 of 32 draws in the first batch and in 5 of 256 in the second, with the same settings and other draws. A two-sided exact test of the two gives P = 0.048. Taken together they are 8 of 288 draws, 2.8 % (1.2 to 5.4 %) (this paper's arithmetic). The table gives the larger sample.
- **At the noise of the 1-THz-class cell the edge lies between three quarters and seven eighths of the set.** At five eighths and at one half no draw of 256 fails (a count, not a rate). At seven eighths the adder fails in 3.9 % of the draws (1.9 to 7.1 %), more often than at the whole set; the two counts, 10 and 7, do not differ by more than chance (two-sided exact test, P = 0.62; this paper's arithmetic). At the noise of the 225-GHz design no draw fails at one half or at three quarters, and no fraction between three quarters and one was run.
- **Every first wrong decision is at a sum pair.** The sum gate takes the majority of three signals of which one is inverted, and it sits at the last clock phase of its stage (design).
- **Read per pair,** the failing share divided by the 53 pairs is 0.52 bad pairs in a thousand at the noise of the 1-THz-class cell, with an interval of 0.21 to 1.05, and 0.37 at the noise of the 225-GHz design (0.12 to 0.85). At three quarters of the set, at the higher noise, the figure is 0.07, from one failing draw, with an interval of 0 to 0.41 (this paper's arithmetic).
- **For a large machine,** if pairs failed independently, a machine of 1,000 pairs would be right in about 60 % of builds at the full set and one of 10,000 pairs in under 1 %, at the noise of the 1-THz-class cell. At the noise of the 225-GHz design the figures are 69 % and 2.5 %. At three quarters of the set they are about 93 % and about half, and these rest on one failing draw (this paper's arithmetic). All of these are point estimates. By the 95 % intervals of the per-pair figure at the full set, a machine of 1,000 pairs would be right in 35 to 81 % of builds at the noise of the 1-THz-class cell and in 43 to 89 % at that of the 225-GHz design. One of 10,000 pairs would be right in 0.003 to 12 % and in 0.02 to 30 % (this paper's arithmetic). The independence is an assumption, and no layout larger than 53 pairs was run with 256 draws.
- **What this does not give** is a budget for a machine of 10,000 pairs. No failure in 256 draws only bounds the failing share below 1.4 %. That needs more draws below three quarters of the set and a larger layout.

8.6 The sensitivity to stray capacitance

The design links pairs through their inductors only. A capacitance between the ends of linked pairs is not part of it, and the model shows what such a stray costs. The case studied is a capacitor of 0.096 fF across each link,

between the like ends of the two pairs, with each pair end padded to ground so that it carries 0.48 fF in all, its link capacitors included. These values are small against the 16 fF of the tank per half: the padding adds 3 % to it. They sit at the far end of the lead at which a pair is driven and read, a short stub of 0.64 fF in all (Section 5.5). In the model the end node of that stub carries 0.08 fF of the 0.64 fF.

Table R16. The serial adder without and with the stray capacitors (in-model). Weakest level of any pair without noise or spread, and runs with a wrong decision, of 32, at the noise of the 225-GHz design with a 3 % spread of the inductance (in one code for the counts). The levels are read with the common reader of the code comparison (Appendix RA), in double precision. Read as in Table R12 they are 204 and 252 mV without the strays and 196 and 187 mV with them.

Supply level	Weakest level, design	Weakest level, with the strays	Failing runs, design	Failing runs, with the strays
0.940 V	205 mV	198 mV	0	0
1.015 V	267 mV	197 mV	0	19

- **At the operating point the strays cost a few per cent of the weakest level. At the top of the supply range they cost a quarter of it,** and the serial adder then fails in 19 of 32 runs where the design fails in none.
- **A second code with the same end capacitances and link capacitors added gives 194 and 198 mV** at the two supply levels. So the second code finds the same effect (in-model, two codes).
- **The added capacitance alone gives about half of the loss, and the coupling alone about a quarter.** This split was measured in the second code at 1.015 V without noise. The added capacitance detunes the tank against the fixed pump. Together the two give the whole loss, which is more than the sum of their parts (in-model, the second code).
- **The sign matters.** In one test with the second code at 1.015 V, without noise, the same coupling with the opposite sign raised the weakest level from 264 to 270 mV (in-model, the second code).
- **With the full set of spreads, whose pump phase error is 10 degrees, the strays make the four-bit adder fail three times as often:** in 21 of 256 draws against 7, at the noise of the 1-THz-class cell (in-model, in one code; a two-sided exact test gives P = 0.01; this paper's arithmetic).

A layout must therefore keep such strays small or count them into the tank. This sensitivity was found when a second code disagreed at 1.015 V, and Appendix RB tells how.

8.7 Which pair errs first, and what other codes find

In the failing runs of the four-bit adder the first wrong decision is most often at a sum pair. That holds for all 23 failing draws of Table R15. It holds for 295 of the 427 failing runs of all lines of the four-bit adder in this Part in which every pair is right without noise, the lines at raised noise and at the noise of the 1-THz-class cell among them (in-model, in one code). The second majority gate comes next with 43, and the carry gate with 32. The remaining 57 are at buffer pairs. In the eight-bit adder the sum pairs begin 51 of 131 failing runs, nearly all of them at raised noise.

The serial adder was also run by the second code at this noise, with the same spread. It is clean at the same supply levels, pump levels and link strengths, with two differences at the edges. At 0.880 V it has 14 wrong sums of 32 where this Part's model has 18. At a 40 % pump it has one wrong sum in one run where this Part's model has none (in-model, two codes; the second code's lines on link strength have 16 runs). No other code ran the four-bit adder at this noise, and none ran the eight-bit adder, the adder on two rails, the accumulator, the single tolerances or the spread budget.

9 Noise

This section gathers the statements of this Part on noise. Sections 7.3, 8.5, 8.6, 10 and 11.3 to 11.5 give further lines at stated noise, and Section 12 refers to it. All results are in-model.

9.1 The noise of the model

The model has two kinds of noise. Every resistor carries its thermal noise at 353 K. The conduction current of every diode carries shot noise with a factor of 1, which is full shot noise (Section 5.5). Both are assumptions. Against the same signal the 1-THz-class cell has 4.78 times the noise power of the 225-GHz design (Section 11.1).

Noise levels are given below as multiples of the noise power of the 225-GHz design. A multiple raises every noise source of the model together.

At the noise of the 225-GHz design the noise is small against the signal. In a row of sixteen without spread, the phase of the last pair but one differs from its noiseless value by 0.3 degrees rms. At 4.78, 16, 64 and 128 times the noise power the figure is 0.7, 1.3, 2.6 and 3.8 degrees (in-model; 127 runs per level). It grows as the square root of the noise power, as a small disturbance does.

9.2 Raised noise without spread

Five layouts were run at raised noise power at the operating point, without any spread of the parts (Table R17).

Table R17. Layouts at raised noise power, without spread, at 0.94 V with a 25 % pump (in-model). Noise power is in multiples of that of the 225-GHz design; the 1-THz-class cell at its own noise is the multiple 4.78. A dash marks a multiple that was not run.

Layout	Runs per multiple	4.78 times	16 times	64 times	128 times	256 times
Row of sixteen	127	none wrong	none wrong	none wrong	none wrong	63 of 889 decisions of pair 14 wrong
Four-bit adder, 53 pairs	64	none wrong	none wrong	none wrong	82 of 1,984 additions wrong, in 45 runs; wrong decisions in 48	694 of 1,984, in all 64 runs
Eight-bit adder, 169 pairs	64; two samples at 16 and 64 times	-	none wrong in either sample	1 of 1,984 additions wrong and wrong decisions in 2 runs, in each sample	192 of 1,984 additions wrong, in 61 runs	1,395 of 1,984, in all 64 runs
Serial adder, 20 pairs	127	none wrong	none wrong	none wrong	30 of 127 sums wrong	123 of 127 sums wrong
Accumulator, 84 pairs	64	none wrong	none wrong	1 of 256 words wrong, in 1 run	97 of 256 words wrong; wrong decisions in 55 runs	233 of 256 words wrong, in all 64 runs

“None wrong” means no wrong decision of any pair in any run: none of 105,152 decisions in the four-bit adder, of 335,296 in each sample of the eight-bit adder, of 78,740 in the serial adder and of 165,760 in the accumulator, per multiple (counts, not rates). For the row it means none of 889 decisions of pair 14 and no first-wrong event.

- **None of the five layouts errs at 16 times the noise power of the 225-GHz design,** without spread. The adder on two rails and rows of 92 were not run at raised noise.
- **At 64 times the eight-bit adder and the accumulator show their first errors:** one wrong addition of 1,984 in the eight-bit adder, in each of two samples of 64 runs, and one wrong word of 256 in the accumulator. The row, the four-bit adder and the serial adder still have no wrong decision.
- **At 128 times every layout with logic fails,** and only the row of sixteen still holds. At 256 times the row fails as well, and every run of the three adders has a wrong decision. The onset is steep: the phase error of a row is 3.8 degrees at 128 times and 46.6 degrees at 256 times.
- **The margin depends on the link strength.** At 64 times the noise power the serial adder with links of 3 % has wrong sums in 125 of 127 runs, and with links of 4.5 % in 30 of 127. With links of 7.5 % and 9 % it has none, as with the 6 % of the design (in-model; 127 runs per value; no spread). With links of 12 % it is wrong even without noise (16 of 20 pairs right). At the noise of the 225-GHz design, with a 3 % spread of the inductance and 32 runs per value, links of 3 to 9 % are clean (Section 8.3).
- **It depends on the input phase as well.** At 64 times the noise power and without spread, a row holds at 12 of sixteen input phases spread over a full turn (64 runs per phase). At the noise of the design, with a 3 % spread of the inductance, it holds at 14 of sixteen (32 runs per phase; Section 7.3). The two lines differ in spread as well as in noise.
- **One other code ran raised noise without spread.** The third code ran the serial adder at 16 times the own noise of the 1-THz-class cell, which is 76 times the noise power of the 225-GHz design. It has 14 wrong decisions of 19,840, all in one run of 32, and no wrong sum at the one output that its check reads (in-model, the third code only). That lies between this Part’s lines at 64 times, with no wrong decision in 127 runs, and at 128 times, with wrong decisions in 52 of 127.

All of these margins are counts, not rates, and all assume full shot noise (Section 9.5).

9.3 The same runs read for the 1-THz-class cell

For the 1-THz-class cell each multiple is divided by 4.78. The column “4.78 times” is that cell at its own noise. The column “16 times” is 3.3 times its own noise, “64 times” is 13 times, and “128 times” is 27 times. So without spread the five layouts show no wrong decision up to 3.3 times the own noise power of the 1-THz-class cell. At 13 times the eight-bit adder and the accumulator show their first errors, and at 27 times every layout with logic fails (in-model; counts, not rates; full shot noise assumed).

9.4 Noise together with spreads

In this Part’s model, runs with spreads of the parts raised the noise to 4.78 times only, which is the 1-THz-class cell at its own noise. Only the second code went further, with one spread (last item below). This is what was found (Sections 8.5 and 11.3).

- **With the full set of spreads (pump phase error 10 degrees) no difference between the two noise levels was found.** The four-bit adder fails in 7 of 256 draws at 4.78 times the noise power, which is 2.7 % (1.1 to 5.6 %), and in 5 of 256 at the noise of the 225-GHz design, which is 2.0 % (0.6 to 4.5 %). A two-sided exact test gives P = 0.77 (this paper’s arithmetic).
- **The single tolerances of the four-bit adder fail first at the same values at both noise levels** (Section 11.3). For the serial adder one line differs: a pump phase error of 30 degrees from pair to pair gives 2 wrong sums of 32 at the noise of the 225-GHz design, without inductance spread, and none at 4.78 times, with a 3 % spread. Several of the paired lines differ in their inductance spread in this way, and every line has 32 runs.
- **At the edges of the working ranges the higher noise costs more.** These lines carry a 3 % spread of the inductance and have 32 runs each. At 0.895 V the four-bit adder has one failing run at 4.78 times the noise power and none at the noise of the 225-GHz design. At a 40 % pump it has 7 failing runs against 3, and at the slot of 38 ps it has 25 against 1. These are the points at which the lowest level without noise has fallen to 34 to 87 mV, against 201 mV at the operating point.
- **One other code went further with one spread.** The second code ran the serial adder with a 3 % spread of the inductance at 16 times the noise power, in 32 runs per line. It has no wrong decision at 0.910 V, from 0.970 to 1.015 V and at pumps of 15 to 35 %. At 0.880 V every run has a wrong sum. At 0.895 V two sums of 32 are wrong, with wrong decisions in 4 runs, and at a 40 % pump nine, with wrong decisions in 16 runs (in-model, the second code only).

So at either carrier the noise of the model is not what limits the design at its operating point, as long as full shot noise is a fair assumption. The spreads are. No run combined the full set of spreads with a noise above 4.78 times. The spread budget of the 1-THz-class cell was therefore run at its own noise and at no higher one.

9.5 The shot-noise factor

Full shot noise is an assumption. In its negative-resistance region an RTD can show more than full shot noise: a factor of up to 6.6 was measured for a GaAs/AlGaAs diode at 77 K [32] (external). No value at room temperature was found, and none for the diode of [4].

A shot-noise factor above 1 multiplies the shot-noise power alone, and a multiple of Table R17 multiplies every source. A run at a multiple N therefore has at least the noise of a 225-GHz design with a shot-noise factor of N, and of a 1-THz-class cell with a factor of N/4.78 (this paper’s arithmetic). This reading holds only one way, and only if more noise in any source never lowers the error count. Without spread the clean runs thus cover a shot-noise factor of up to 16 in the 225-GHz design and of up to 3.3 in the 1-THz-class cell. The runs at four times those multiples, where the first errors appear, raise the thermal noise as well. They do not show at which shot-noise factor errors would begin.

With the full set of spreads (pump phase error 10 degrees) only the four-bit adder was run with 256 draws, at 1 and at 4.78 times the noise power, and it fails in 5 and in 7 of 256 draws there. So the spread budget, with that failing share, covers a shot-noise factor of up to 4.78 in the 225-GHz design and of 1 in the 1-THz-class cell. A shot-noise factor above 1 together with the full set of spreads was not run for that cell (Section 14).

9.6 Counts are not rates

Every zero of this section is a count. The largest line without a wrong decision at 16 times the noise power has 335,296 decisions. If decisions were independent, that zero would bound the rate to at most 1.1×10^{-5} per decision, the upper end of the exact 95 % interval, at that raised noise (this paper's arithmetic). No rate at the physical noise is claimed, and no extrapolation from raised noise was made. The pass line of 6.3×10^{-9} per cell decision that Part III derives for its lane (Part III, Section 5.2; in-model there, an upper bound) is quoted for scale only. The counts of this Part cannot reach it.

9.7 Quantum noise

The model is classical. The quantum of the carrier, expressed as a temperature hf/k, is 10.8 K at 225 GHz and 51.6 K at 1.075 THz, against 353 K (this paper's arithmetic). Part II takes "T_Q = ħω₀/k_B ≈ 48 K" as the crossover at 1 THz (Part II, Section 3.2). No quantum noise floor and no noise figure were computed.

10 Assumptions and faster carriers

The diode of the 225-GHz design rests on three assumed values: its delay, its contact resistance and the shape of its curve (Section 5.2). This section varies the first two and some values of the circuit, and then asks how far the same diode pair carries when the tank is tuned to other carriers. All results are in-model. The rows of sixteen carry a 3 % spread of the inductance and the noise that belongs to their carrier, with full shot noise assumed, and have 32 runs per supply level in steps of 15 mV. Section 11 treats the 1-THz class.

10.1 The assumed values

Table R18. Variants of the 225-GHz pair in what is assumed: the supply range over which the pair oscillates by itself, and the range over which a row of sixteen holds at a 25 % pump (in-model). One value is changed at a time and the tank is tuned again to the carrier. Each scan covers eleven supply levels; "end" marks a range that ends with its scan.

Changed value (the design has)	Oscillates by itself	Row holds at
Diode delay 50 fs (100 fs)	0.97 to 1.14 V	0.880 to 1.015 V, end
Diode delay 200 fs	0.97 to 1.12 V	0.895 to 1.015 V, end
Diode delay 300 fs	0.98 to 1.10 V	0.905 to 1.025 V, end
Contact 6 Ω per diode (12 Ω)	0.93 to 1.11 V	0.855 to 0.975 V, end
Contact 24 Ω per diode	1.04 to 1.17 V	0.950 to 1.085 V, end
Coupling of the two halves of the inductor 0.1 (0.3)	0.97 to 1.14 V	0.880 to 1.015 V, end
Coupling of the two halves 0.5	0.97 to 1.14 V	0.880 to 1.015 V, end
Supply source 5 Ω (2.5 Ω)	1.00 to 1.15 V	0.910 to 1.045 V, end
Capacitance of the supply node four times	0.97 to 1.14 V	0.880 to 1.015 V, end

- **Rows hold for diode delays from 50 to 300 fs and for contacts from half to twice the assumed value,** over 120 mV of supply level or more in every case. With pumps of 20 and 30 % they hold as well, over 90 mV or more at 20 %.
- **The working range moves with the pair's own threshold.** With a contact of 24 Ω the pair oscillates by itself only from 1.04 V, and the row holds from 0.950 V. With 6 Ω both lie lower. The rule of the design is therefore "just below the pair's own threshold", and 0.94 V is its value for this diode.
- **Adders were not run on these variants.** The statements of Section 8 are for the design values.

10.2 The same diode pair at other carriers

The junction of 2.5 fF and the contact of 12 Ω were kept, and the tank was tuned to other carriers with the pump at twice each carrier and a slot of 15.6 carrier periods. Each pair was run at the noise that belongs to its carrier.

Table R19. The diode pair of the 225-GHz design tuned to other carriers: supply levels at which a row of sixteen holds at a 25 % pump (in-model). Each scan covers eleven levels around the pair's own threshold; "end" marks a range that ends with its scan. The level is that of pair 14 in the middle of the range.

Carrier	Pump	Diode delay	Row holds at	Level
160 GHz	320 GHz	100 fs	0.865 to 1.015 V, the whole scan	200 mV
320 GHz	640 GHz	100 fs	0.910 to 1.015 V, end	184 mV
450 GHz	900 GHz	100 fs	0.935 to 0.995 V	152 mV
640 GHz	1.28 THz	100 fs	0.975 to 0.990 V	78 mV
450 GHz	900 GHz	35 fs	0.925 to 0.985 V	171 mV
640 GHz	1.28 THz	35 fs	0.950 to 0.965 V	90 mV
900 GHz	1.8 THz	35 fs	0.960 to 0.990 V	89 mV
1,075 GHz	2.15 THz	20 fs	none	

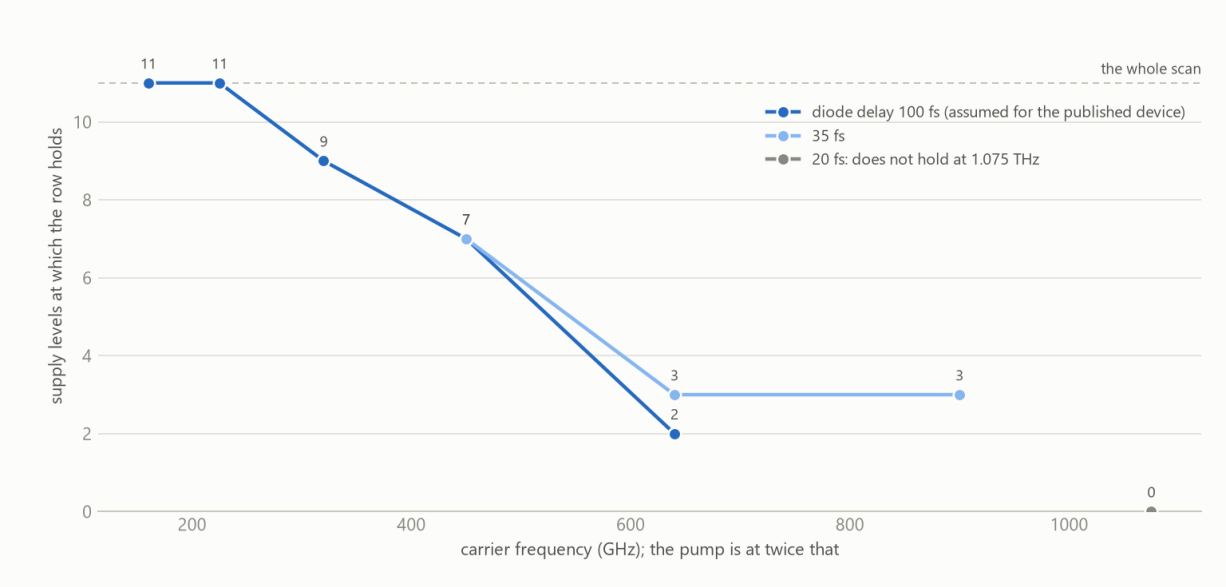


Figure R7. The diode pair of the 225-GHz design tuned to other carriers: number of supply levels, of eleven that are 15 mV apart around each pair's own threshold, at which a row of sixteen holds (in-model; a 3 % spread of the inductance; the noise of each carrier; the aligned input phase; 32 runs per level; the widest unbroken range among pumps of 20, 25 and 30 %). The value at 225 GHz is cut to the same eleven levels. Table R19 gives the 25 % pump only, so at 320 and 450 GHz, and at 640 GHz with 35 fs, the figure counts more levels.

- **With the assumed delay of 100 fs the pair carries a row up to 640 GHz.** The range narrows from the whole scan at 160 GHz to two levels 15 mV apart at 640 GHz, and the level falls from 200 to 78 mV.
- **With a delay of 35 fs it carries a row at 900 GHz,** over 30 mV.
- **At 1.075 THz it carries none,** even with a delay of 20 fs. The junction of 2.5 fF is then most of the tank. Section 11.5 shows which smaller junctions or better contacts would do.
- **At the highest carriers the input phase matters.** At 640 GHz with the 100-fs diode and at 900 GHz the row holds at no supply level when the input lies a quarter of π of pump phase before the aligned value.

10.3 Adders at the other carriers

The four-bit adder was run on the same pairs, each at one supply level and one pump level inside the range of its row, at the noise of its carrier (Table R20).

Table R20. The four-bit adder on the diode pair of the 225-GHz design tuned to other carriers (in-model; 32 runs per line). Wrong additions of 992 and, in brackets, runs with a wrong addition. “Seven spreads” are those of Section 7.2 with a pump phase error of 10 degrees.

Carrier	Diode delay	Supply and pump level	Inductance spread 3 %	Seven spreads at once	Lowest level without noise
160 GHz	100 fs	0.940 V, 25 %	0	0	212 mV
320 GHz	100 fs	0.955 V, 30 %	0	0	200 mV
450 GHz	100 fs	0.950 V, 30 %	0	26 (7)	145 mV
640 GHz	100 fs	0.975 V, 30 %	117 (20)	273 (30)	73 mV
450 GHz	35 fs	0.955 V, 30 %	0	0	187 mV
640 GHz	35 fs	0.950 V, 30 %	0	109 (24)	78 mV
900 GHz	35 fs	0.975 V, 25 %	72 (21)	356 (30)	76 mV

- **With the assumed delay of 100 fs the four-bit adder is clean up to a 450-GHz carrier** with an inductance spread of 3 %, and up to 320 GHz with seven spreads at once, whose pump phase error is 10 degrees here. At 450 GHz the seven spreads give wrong additions in 7 of 32 runs.
- **At 640 GHz it fails with the assumed diode,** although a row still holds there. With a delay of 35 fs it is clean at 640 GHz with the 3 % spread and fails with seven spreads.
- **At 900 GHz it fails even with a delay of 35 fs,** in 21 of 32 runs with the 3 % spread.
- **Logic asks more of a pair than a row does.** A row holds where its pair 14 keeps 78 to 90 mV. With the 3 % spread the four-bit adder is clean where its weakest pair keeps 145 mV or more without noise, and on one line with 78 mV. With seven spreads it is clean only at 187 mV and above, and at 145 mV it fails in 7 of 32 runs.

The serial adder gives the same picture, in two samples of 32 runs per line (in-model; counts, not rates; the seven spreads as in Table R20). With the assumed diode it has no wrong sum at 160, 320 and 450 GHz, with the 3 % spread and with seven spreads; at 450 GHz with seven spreads one sample has two wrong decisions in one run. At 640 GHz it has wrong sums in 18 and in 10 of the 32 runs with the 3 % spread, and in 18 and 24 with seven spreads. With a delay of 35 fs it has none at 450 GHz, and none at 640 GHz with the 3 % spread. With seven spreads it has 5 and 9 of 32 at 640 GHz. At 900 GHz it has 10 and 14 of 32 with the 3 % spread, and 19 and 21 with seven spreads.

10.4 The pumps these carriers would need

Carriers of 320, 450, 640 and 900 GHz need pumps at 0.64, 0.9, 1.28 and 1.8 THz, locked to the input reference and delivered to the supply node of every pair. The pump power per pair was worked out for the 225-GHz design, for a 160-GHz pair and for the 1-THz-class cell (Sections 2.4 and 11.6), not for the carriers of this section. The powers found for sources near those frequencies are these (external).

- **Near 0.65 THz:** 1.14 mW at 0.650 THz from one RTD in a rectangular cavity [9] (abstract, which does not say whether the operation was continuous).
- **Near 0.9 THz:** about 0.24 mW at about 925 GHz from two coupled RTDs [10] (abstract), and 73 µW at 863 GHz from one RTD with a slot antenna [12] (abstract). The group of [10] measures power with a pulsed bias at 50 % duty (the first author’s thesis, read in part).
- **Near 1 THz, the nearest band with several reports:** 0.73 mW from an array of 89 RTD elements that are not intentionally coupled, in pulsed operation, and 21 µW from single oscillators [11] (abstract). A silicon chip with 42 radiators gives 80 µW at 1.013 THz [36]. A multiplier chain that is not on a chip gives 2 mW at 1.03 THz [37] (abstract).
- **Near 1.3 THz:** no source was found at that frequency. The nearest figures above it are 0.4 µW at 1.55 THz from an RTD [15] and 0.7 mW at 1.64 THz from a multiplier chain off the chip [37] (abstract).
- **Near 1.8 THz:** 2.2 µW at 1.74 THz from an RTD [17], and more than 20 µW over most of 1.80 to 2.04 THz from a multiplier chain off the chip [35].

None of these sources has been shown to deliver its power to a supply node, to hold a set phase against a reference at half its frequency, or to feed four clock phases with stepped pump phases. Appendix RC compares these readings with the figures that Part III quotes for RTD oscillators near 1 THz.

11 A 1-THz-class specification

This section takes the second step of the request: the same design at a carrier of 1.075 THz, and what it would ask of the diode and of the pump. It says in what sense the specification is validated: in the model, and in no other sense.

11.1 The step is a change of units

Divide every time of the 225-GHz design by K = 4.78, and with it every capacitance and inductance. Resistances, voltages and currents stay. Without noise, the equations of Section 5.5 are then unchanged, term by term. The model in fact runs in these scaled units, and the 225-GHz design and the 1-THz-class cell are one calculation read in two sets of units. The step is exact for the model's equations (this paper's arithmetic). Listing r5 of the package runs two linked pairs in both sets of units, with the noise of the 225-GHz design scaled into each, and gives the same traces to 10^{-13} of the signal (demonstrated (runnable)).

One thing does change: the noise. A capacitance that is 4.78 times smaller has 4.78 times the thermal noise power, and the shot noise acts over a bandwidth that is 4.78 times larger. Against the same signal the 1-THz-class cell has 4.78 times the noise power of the 225-GHz design, with full shot noise assumed at both. Every run of Sections 7 and 8 is therefore also a run of the 1-THz-class cell at about a fifth of its own noise, and the cell has to be run again at its own noise. Section 11.3 does that.

What the step does not cover. Everything the model leaves out must shrink by the same factor: supply paths, the pump and clock planes, pads, losses in the metal, radiation and heat. None of these was modelled. One example by arithmetic: a supply error of 14 mV is 1.5 % of the supply level. To keep it under edges of 3 ps at 10.5 mA, the supply path of a pair must stay below about 4 pH by the mean slope of the edge, and below about 2.6 pH by its steepest slope (this paper's arithmetic). The quantum of the carrier grows as well: hf/k is 51.6 K at 1.075 THz against 10.8 K at 225 GHz, and the noise of the model is classical (this paper's arithmetic; Section 9.7).

11.2 The specification

Table R21. The 1-THz-class cell (design, except the power per pair, which is in-model; the values of Table R3 with every time, capacitance and inductance divided by 4.78). The values not listed here are those of the column "The 1-THz-class cell" of Table R3.

Quantity	Value
Carrier; pump	1.076 THz; 2.152 THz at 25 % of the supply level
Slot	14.5 ps (69 GHz); four clock phases; edges of 3 ps
Diode, per diode	peak 6.35 mA, valley 2.85 mA, 0.55 V between them
Junction capacitance, per diode	0.52 fF
Diode delay	21 fs
Contact resistance, per diode	12 Ω
Tank, per half	3.35 fF with the junction; 5.5 pH in the antiphase mode; quality factor 4
Link	0.33 pH in magnitude
Supply level	0.94 V
Power per pair	7.2 mW (in-model)

The slot of 14.5 ps equals the slot of Part III's lane, which Part III uses at a frontier of 69 GHz that is "neither confirmed nor moved (open)" (Part III, Section 2.2). It is equal by choice of the carrier and is not borrowed as support.

The same relative spreads are tighter absolute ones. The runs of Section 11.3 apply the spreads of Section 8 as fractions. In this cell 3 % of the inductance is 0.17 pH, a clock timing error of 2 % of the period is 0.29 ps, and 10 degrees of the pump wave are 13 fs (this paper's arithmetic).

11.3 The adders at the cell's own noise

The four-bit and the serial adder were run again at 4.78 times the noise power, over supply level, pump level, link strength and slot, and with every single tolerance on top of a 3 % spread of the inductance (in-model, in one code; 32 runs per line).

Table R22. The adders at the 1-THz-class cell's own noise (in-model, in one code; 32 runs per line; a 3 % spread of the inductance in every line; full shot noise assumed). Wrong additions of 992, or wrong sums of 32. In brackets are the runs with a wrong addition for the four-bit adder, which in these lines are also its runs with a wrong decision, and the runs with a wrong decision of any pair for the serial adder.

Condition	Four-bit adder	Serial adder
Operating point	0	0
Supply 0.880 V	473 (32)	30 (32)
Supply 0.895 V	1 (1)	0
Supply 0.910, 0.970, 0.985, 1.000 and 1.015 V	0 at each	0 at each
Pump 15, 20, 30 and 35 %	0 at each	0 at each
Pump 40 %	22 (7)	1 (3)
Links 3, 4.5, 7.5 and 9 %	0 at each	0 at each
Links 12 %	wrong without noise	wrong without noise
Slot 8 ps	52 (25)	not run
Slots 10, 12 and 17 ps	0 at each	0 at each
Supply level error 1, 1.5 and 2 %	0 at each	0 at 1 and 2 %
Supply level error 3 %	18 (5)	2 (3)
Damping resistor spread 5 and 10 %	0 at each	0 at each
Damping resistor spread 15 %; 20 %	22 (6); 100 (14)	not run; 8 (10)
Pump phase error from pair to pair 10 and 20 degrees	0 at each	0 at each
Pump phase error from pair to pair 30 degrees	7 (2)	0
Pump phase error of a clock phase 5, 10 and 20 degrees	0 at each	0 at each
Link strength error 10 %	0	0
Link strength error 20 %	133 (21)	7 (12)
Clock timing error 2 and 5 %; pump level error 20 %; diode current 10 %; difference inside a pair 5 %	0 at each	0 at each
Input phase 0.125π and 0.25π of pump phase either way from the aligned value	0 at each	0 at each

- **At its own noise the cell loses at most one step of each working range, and it fails more often at the edges.** The four-bit adder is clean at the levels run from 0.910 to 1.015 V and has one failing run of 32 at 0.895 V, where it is clean at the lower noise. At a 40 % pump it has 7 failing runs against 3. The serial adder is clean from 0.895 to 1.015 V. At a 40 % pump it has one wrong sum, where it has none at the lower noise (counts, not rates).
- **It keeps the first values at which the tolerances are no longer clean.** A link strength error of 20 % fails in both adders at both noise levels, and a supply level error of 3 % in the four-bit adder. In the serial adder a supply level error of 3 % now gives 2 wrong sums of 32. At the lower noise it gave no wrong sum, and one run had a wrong decision at a pair that reaches no output. A damping resistor spread fails at 15 % in the four-bit adder and at 20 % in the serial adder, on which 15 % was not run. In the four-bit adder a pump phase error of 30 degrees from pair to pair fails as well.
- **One line differs the other way.** The serial adder, which had two failing runs at a pump phase error of 30 degrees at the lower noise, has none here. The two sets of lines carry different draws. At the lower noise the lines on the pump phase from pair to pair, the link strength error, the clock timing, the pump level error, the diode current and the difference inside a pair have no inductance spread. Here every line has a 3 % spread.
- **The short slot suffers most.** At 8 ps, which is 38 ps in the 225-GHz design, the four-bit adder fails in 25 of 32 runs, against one of 32 at the lower noise.
- **With the full set of nine spreads,** whose pump phase error is 10 degrees, the four-bit adder fails in 7 of 256 draws at this noise, which is 2.7 % (1.1 to 5.6 %). With 32 draws it fails in 1 of 32, and the serial adder in none of 32 (Section 8.5; counts, not rates).

The eight-bit adder and the accumulator were run at this noise at fewer points. The lines are an inductance spread of 3 % or 5 %, half of the full set of spreads, with every spread halved and a pump phase error of 5 degrees, and supply levels of 0.910 and 0.970 V with a 3 % spread. In all of them the eight-bit adder has no wrong addition of 992 and the accumulator no wrong word of 128. The accumulator is also clean at pumps of 20 and 30 % (in-model, in one code; 32 runs per line, and a second sample of the eight-bit adder's first three lines with the same result; counts, not rates). Neither layout was run with the whole of the full set (10 degrees) at this noise.

The noise margin is smaller than that of the 225-GHz design by the same factor of 4.78 (this paper's arithmetic). Section 9 gives the noise powers up to which each layout was run without error. Read for this cell, each of them is divided by 4.78. Both noise levels assume thermal noise at 353 K and full shot noise.

11.4 What "validated in the model" covers

Is the specification validated? In the model, within the lines run, yes; in no other sense. "Within the lines run" has three limits. With the full set of nine spreads, whose pump phase error is 10 degrees, the four-bit adder fails in 7 of 256 draws at this noise (Section 8.5). That set was not run on the eight-bit adder or on the accumulator at this noise. And a shot-noise factor above 1 was not run together with the full set of spreads (Section 9.5). The model itself was tested in two ways: by other codes, and by checks of time step, stub grid and precision (Appendix RA).

Three further codes of the circuit were written from specifications alone (Appendix RA). The second was written in four stages for the 225-GHz design and is read here through the change of units, at 4.78 times its noise. The third and the fourth were each written by one modeller from a stand-alone specification in the units of this cell, with the noise derived from the thermal and shot-noise powers directly.

Table R23. Four codes at the 1-THz-class cell's own noise (in-model; a 3 % spread of the inductance; 32 runs per line, 16 for the third code). Serial adder: wrong sums and, in brackets, runs with a wrong decision.

Condition	This Part's model	Second code	Third code	Fourth code
Supply 0.880 V	30 (32)	24 (31)	13 (16)	not run
Supply 0.895 to 0.985 V	0	0	0	0 at 0.94 V, the only level of this band that it ran
Supply 1.000 V	0	0	0	0
Supply 1.015 V	0	0	0	1 (1)
Pump 15 and 35 %	0	0	0	not run
Pump 40 %	1 (3)	5 (7)	5 (6)	not run
Links 3 to 9 %	0	0	not run	not run

- **The serial adder rests on four codes and rows of sixteen on three, within the lines each ran.** The three codes that ran these lines agree that the serial adder is clean from 0.895 to 1.000 V and fails at 0.880 V. The fourth ran 0.94, 1.000 and 1.015 V and is clean at the first two. It ran no row of sixteen.
- **The four-bit adder rests on two.** The fourth code ran it at four supply levels: no wrong addition of 992 at 0.895, 0.940 and 1.000 V, and 4 wrong additions in 2 runs of 32 at 1.015 V. This Part's model has one wrong addition at 0.895 V and none at the other three. The fourth code's author noted that at 0.895 V some sum pairs read only a few millivolts under noise without a wrong decision, a thin margin that the rule of a quarter turn does not show.
- **At the edges the codes differ, and the differences are not explained.** At a 40 % pump, wrong sums are 1 of 32 in this Part's model, 5 of 32 in the second code and 5 of 16 in the third. Runs with a wrong decision are 3 of 32, 7 of 32 and 6 of 16. This Part's model fails least often there. Rows of sixteen show no wrong decision from 0.895 V in this Part's model and from 0.880 V in the second and the third code. The third code has six wrong decisions in one run of 16 at 1.030 V, a level at which this Part's model was not run at this noise.
- **Everything else rests on this Part's model alone.** Among it are every single tolerance, the full set of spreads, the eight-bit adder, the accumulator, the lines on the slot, and the diode region below.
- **The two new codes take their noise from first principles in the cell's own units.** Where the third code and the second both fail, at 0.880 V and at a 40 % pump, their counts are within the scatter of 16 or 32 runs. The fourth code ran no line at which the second code fails.

No code can validate what all four leave out: the pump, the clock, the wires and the diode itself.

11.5 What the diode must be

The exact cell has a junction of 0.52 fF, a delay of 21 fs and a contact of 12 Ω at a peak current of 6.35 mA. That is one point. To learn how far a diode may lie from it, pairs were tuned to the same carrier with larger junctions, longer delays and other contacts, always with the same currents. They were run as rows of sixteen at the noise of a 1.075-THz cell (in-model, in one code; 32 runs per supply level; a 3 % spread of the inductance).

Table R24. Pairs for a 1.075-THz carrier with other diodes: supply range over which a row of sixteen holds at a 25 % pump (in-model, in one code; a 3 % spread of the inductance; the noise of a 1.075-THz cell; 32 runs per supply level). “None”: the row holds at no supply level of the scan. Ranges that end at 1.015 or 1.085 V end with their scan.

Junction per diode	Contact 12 Ω, delay 21 fs	12 Ω, 35 fs	12 Ω, 50 fs	Other contacts, delay 35 fs
0.52 fF	0.895 to 1.015 V	0.895 to 1.015 V	0.895 to 1.015 V	24 Ω: 0.965 to 1.085 V
0.80 fF	0.910 to 1.015 V	0.910 to 1.000 V	0.920 to 1.010 V	24 Ω: 0.990 to 1.080 V
1.25 fF	0.940 to 0.985 V	0.950 to 0.980 V	0.950 to 0.980 V	24 Ω: 1.045 to 1.060 V
1.70 fF	0.950 to 0.965 V	0.965 V only	0.975 to 0.990 V	6 Ω: none at 25 %; 0.910 to 0.925 V at a 30 % pump
2.50 fF	none	does not oscillate	does not oscillate	6 Ω: 0.905 to 0.950 V, and 0.980 V alone; 3 Ω: 0.875 to 0.935 V

- **Rows hold up to a junction of 1.25 fF at any delay from 21 to 50 fs,** over 30 to 45 mV of supply level, against at least 120 mV for the exact cell, whose range ends with its scan (all at a 25 % pump).
- **The serial adder is clean on those pairs.** With junctions of 0.52, 0.80 and 1.25 fF at delays of 21, 35 and 50 fs it gives no wrong sum in 32 runs with a 3 % spread of the inductance, except one wrong sum in one run at 1.25 fF and 50 fs. With half of the full set of spreads, where the pump phase error is 5 degrees, all nine pairs are clean. Each was run at one supply level inside its range and at one pump level, 30 % for most (in-model, in one code; 32 runs; counts, not rates).
- **Pairs with a junction of 1.7 fF fail logic** although their rows hold over one or two supply levels at a 25 % pump. With the 3 % spread the serial adder has wrong sums in 13 to 30 of 32 runs, and with half of the full set (5 degrees) in 1 to 29.
- **A junction of the present size, 2.5 fF, works only with a smaller contact.** With 12 Ω the pair does not oscillate or holds nowhere. With 6 Ω or 3 Ω a row holds over 45 to 60 mV.

The four-bit adder was run on the same pairs, at the same supply and pump levels, with a 3 % spread of the inductance and with half of the full set of spreads (5 degrees) (in-model, in one code; 32 runs per line; counts, not rates). No pair with another diode was run with the whole of the full set (10 degrees).

- **With junctions of 0.52, 0.80 and 1.25 fF the four-bit adder is clean at every delay from 21 to 50 fs** with the 3 % spread. With half of the full set (5 degrees) it has one wrong addition of 992 on two of the nine pairs and none on the others.
- **With a junction of 1.7 fF it fails at every delay,** in 24 to 32 of 32 runs with the 3 % spread, and with a contact of 6 Ω as well. These pairs were run at the lower edge of their narrow ranges. Their weakest pair then reaches only 3 to 72 mV without noise, against 113 to 205 mV on the nine pairs above. Why the gates of these pairs come up so weak while their rows hold was not found (open).
- **With the present junction of 2.5 fF it is clean with a contact of 3 Ω** and fails with 6 Ω, in 18 of 32 runs.
- **The smaller junctions work with a contact of 24 Ω:** the adder is clean with 0.52 and 0.80 fF. With 1.25 fF it fails in 26 of 32 runs. That line, however, was run at 1.045 V with a 20 % pump, one step below the only level at which its row holds with that pump, so it is not a fair test of that pair.
- **Contact and junction act together.** At a fixed carrier the loss that a contact adds to the tank goes as the contact resistance times the square of the junction capacitance (this paper’s arithmetic). Every pair on which the four-bit adder is clean has 19 Ω fF² or less, and every pair with 35 Ω fF² or more fails or does not hold a row. One pair does not fit: 1.7 fF with 6 Ω has 17 Ω fF² and fails.

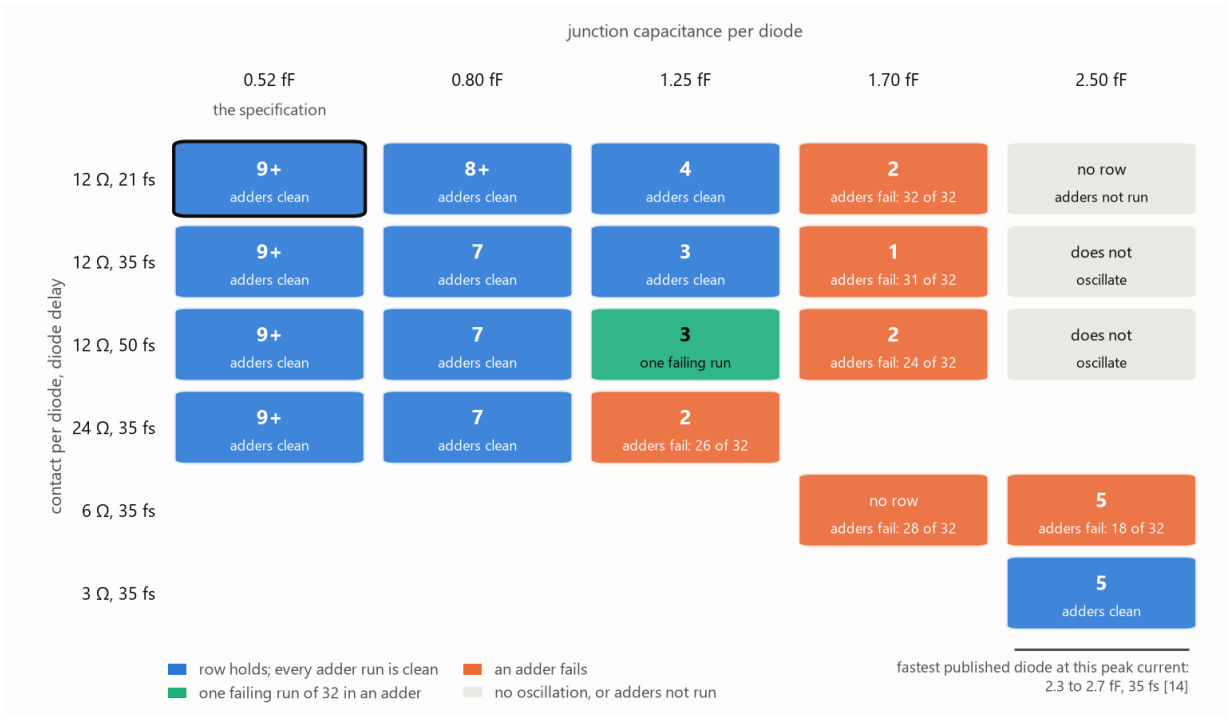


Figure R8. Pairs for a 1.075-THz carrier with other diodes (in-model, in one code; a 3 % spread of the inductance; noise of the 1-THz-class cell; 32 runs per line). The number in a box is the number of supply levels, 15 mV apart, at which a row of sixteen holds at a 25 % pump; a plus marks a range that ends with its scan. The colour gives the worse of the four-bit and the serial adder on that pair with the 3 % spread, each run at one supply level and one pump level; pairs with a contact other than 12 Ω have the four-bit adder only. With half of the full set of spreads (pump phase error 5 degrees), the pairs at 0.52 fF and 50 fs and at 1.25 fF and 35 fs have one failing run of 32 each. The adder of the pair with 1.25 fF and 24 Ω was run one step outside the range of its row. The framed box is the specification of Table R21. The bar marks the capacitance that the fastest published diode would have at the peak current of the cell [14] (this paper's arithmetic).

Against published diodes. One review lists, for the diode of the oscillator with the highest fundamental found, 1.98 THz, a peak current density of 31 mA/µm², a capacitance of 13 fF/µm² and a delay of 35 fs [14] (external). Its delay is the dwell time plus half the transit time, which is the quantity that the model calls the diode delay. The table of the review does not say how the capacitance was obtained, and beside one of its figures the review takes 2.4 fF for a diode of 0.21 µm², which is 11.4 fF/µm².

- **The delay is within reach on this reading.** Logic held with delays up to 50 fs, with one failing run of 32 on two of the 50-fs lines, and 35 fs is published [14]. A thesis fits intrinsic delays of 20 and 35 fs, and total delays of 100 and 90 fs, for two diodes that oscillate at 1.47 and 1.86 THz [15] (external). Of the two, the intrinsic delay is the model's diode delay.
- **The current per capacitance is not.** The published diode has 2.4 mA of peak current per fF (this paper's arithmetic). Its capacitance can be read in two ways. Read as the total one, it stands against the junction of a pair plus the share that the delay brings. That share is the magnitude of the diode's slope times its delay: 0.2 to 0.7 fF for slopes of 9.5 to 13.8 mS and delays of 21 to 50 fs. The pairs on which logic still held then ask 3.3 to 4.4 mA per fF, about 1.4 to 1.8 times as much, and the exact cell asks 8 to 9, which is 3.3 to 3.7 times. Read as the junction alone, the figures are 5 and 12 mA per fF: 2.1 times and 5 times.
- **A diode of slower oscillators does better on that one figure.** For RTD oscillators at 0.4 to 0.8 THz a preprint gives 12 mA/µm² and assumes 3.3 fF/µm², a value that it states was verified by test measurements. That is 3.6 mA per fF [16] (external, a preprint; this paper's arithmetic). Against it the pairs on which logic still held ask 0.9 to 1.4 times, and the exact cell 2.2 to 3.4 times, on the two readings. At the peak current of the cell it would have a junction of about 1.7 fF, the size at which the adders fail in the model (this paper's arithmetic). Its delay is not in what was read, so it is not known to combine that figure with the delay that the cell needs.
- **The contact is at the edge or beyond it.** The model does not fix the area of the cell's diode. At the current densities of the two fastest diodes, 31 to 50 mA/µm² [14], a diode of 6.35 mA has 0.13 to 0.20 µm², and the 12 Ω of the cell are 1.5 to 2.5 Ω µm². At the capacitance per area of the fastest diode, 11.4 to 13 fF/µm²

[14], a junction of 0.52 fF has 0.04 to 0.05 μm², and the 12 Ω are about 0.5 Ω μm² (this paper's arithmetic). A thesis reports contacts as low as 2 to 3 Ω μm² with a strained cap layer [13], and 15 Ω μm² was measured in the group with the fastest oscillators [15] (external). On the first reading the contact of the cell is at or below the best reported figure. On the second it is four to six times below it.

- **The route with the present junction asks even more of the contact.** At the peak current of the cell the published diode would have 2.3 to 2.7 fF, close to the present 2.5 fF. Its 2.4 mA per fF is what this route asks: 2.2 mA per fF of total capacitance, or 2.5 of junction alone (this paper's arithmetic). But with 2.5 fF a row holds only with a contact of 6 Ω or 3 Ω, and the four-bit adder is clean only with 3 Ω. At the 0.19 to 0.22 μm² of such a junction that is about 0.6 Ω μm², a third to a fifth of the best reported figure (this paper's arithmetic).
- **No published diode combines the figures of either route.**

11.6 What the pump must be

The pump must run at 2.15 THz, in step with the carrier. Its rms phase error from pair to pair may be at most 10 to 20 degrees of the pump wave: rows hold at 10 degrees, and the adders are clean at 20 (in-model; Sections 7.3 and 8.4). Ten and twenty degrees at 2.15 THz are 13 and 26 fs (this paper's arithmetic). The pump term of 235 mV and the pump current of 6.1 mA per pair, almost all reactive, are 0.72 mVA. Through a resonant feed with a quality factor of 5 to 10 the pump must deliver about 0.07 to 0.15 mW of real power per pair (this paper's arithmetic; Section 2.4).

No published source does this. Near 2 THz the powers found are these (external). A quantum-cascade laser source by difference-frequency generation gives 0.6 μW at 2.06 THz in continuous operation at room temperature, the lower end of its tuning range [34]. A chain of frequency multipliers, not on a chip, gives 60 μW at 1.95 THz and stops near 2.04 THz [35]. RTD oscillators give 2.2 μW at 1.74 THz [17] and 0.4 μW at 1.92 THz ([8], abstract; the power from the thesis [13], secondary, and not stated as continuous). Nothing was found at 2.15 THz. Against 0.1 mW per pair the two sources on a chip at 1.92 and 2.06 THz are about 170 to 250 times short (this paper's arithmetic). The one report found of an RTD oscillator locked by a signal at half its frequency is at about 550 GHz [28]. Part III's own check "found no injection-locking or phase-noise data for resonant-tunnelling diodes at 0.8–1.2 THz" (Part III, Section 8.1(e); external there).

The pump is therefore the part of the specification that is furthest from anything published. The specification is validated in the model only, and the model's pump is an ideal source.

12 Energy, throughput and a conditional outlook

The second request set power and cost aside. This section reports them all the same, briefly, because they bound what the third request asks for: a statement of where the approach could lead.

12.1 Energy and throughput

A pair draws 10.5 mA while it is on and 7.2 mW on average (in-model). Almost all of that is the direct current of its two diodes; the stored signal energy is under a femtojoule (in-model, one pair). Per pair and slot that is 0.50 pJ in the 225-GHz design and 0.10 pJ in the 1-THz-class cell (this paper's arithmetic). An eight-bit addition, 169 pairs for one slot, costs about 84 pJ in the 225-GHz design and about 18 pJ in the 1-THz-class cell, before the pump (this paper's arithmetic).

These figures leave out the pump. At the efficiency of Canon's array at 450 GHz, about 1 % [4], a pump power of 0.07 to 0.15 mW per pair would cost 7 to 15 mW of supply, one to two times the pair's own power (external; this paper's arithmetic). No source near 2 THz with such an efficiency is known. The laser sources by difference-frequency generation, the kind that reaches 2.06 THz [34], have a wall-plug efficiency of 0.8×10^{-6} in continuous operation, in a review whose continuous-wave figure is at 3.4 THz [33] (external).

Throughput. A ripple-carry adder of this kind takes a new pair of operands in every slot (design). Its rate is the clock rate: 14.4 billion eight-bit additions per second in the 225-GHz design and 69 billion in the 1-THz class (this paper's arithmetic). Part I states "one addition per 4-ps slot (2.5×10^{11} additions/s, wave-pipelined) as the design baseline" for its half adder. It finds in its model that logic with a fan-out of two does not close at that slot once cavity ring-down is booked. With a launch confined to its slot and gated by the data it closes at about 69 GHz, in a band of 63 to 74 GHz. That figure is neither confirmed nor moved when the bias is set as a ratio to

the solver's threshold (Part I, abstract; in-model there). The two rates count different things, additions of eight bits here and of one bit there, and are not set against each other.

12.2 Against the figures of the earlier Parts

Part I's table of platforms books RTD oscillators and latches at about a femtojoule per operation and transistor logic at attojoules to femtojoules, with the caption that its "Energy figures are order-of-magnitude and not normalized for function" (Part I, Section 2). The pair's 0.50 pJ per slot is about 500 times that entry for RTDs, and its 0.10 pJ in the 1-THz class about 100 times (this paper's arithmetic). This Part makes no energy comparison of its own with transistor logic.

The released chain of Parts I to III books a cell dissipation of 12.67 μW at the 353 K cap at its hydrodynamic tier, with an upper bound of 16.64 μW. With its kinetic correction it books 15.9 to 16.7 μW. Both rest on a lifetime that Part I states as a best case (Part III, Section 2.2). The pair takes 430 to 570 times that power, before its pump (this paper's arithmetic). That compares a model result with a booked figure of another model, not with a measured cell. Part I calls the fabric-side energy of its half adder, 0.35 to 0.5 fJ per addition at the 4-ps slot without the photonic drive chain, "CMOS-class, not below it" (Part I, Section 8.1). The fabric of pairs starts far behind that, although the two figures count different things, a pair per slot and a half adder per addition (this paper's arithmetic).

12.3 Power density and heat

The power per pair stays at 7.2 mW when the carrier rises, while the passive parts shrink. A pair of the 225-GHz design on an assumed footprint 20 to 50 μm wide dissipates 0.3 to 1.8 kW/cm² if pairs are packed; no layout was drawn. In the 1-THz class the density is 4.78 to 23 times that, about 1.4 to 41 kW/cm² (this paper's arithmetic). One watt runs about 140 pairs at either carrier, and the eight-bit adder dissipates 1.2 W (this paper's arithmetic).

Heat was not modelled. On these figures it binds unless the pairs are spread out, and the cap of 80 °C of the series is neither met nor tested. The gains of a faster carrier are therefore gains in energy per decision and in throughput per watt, not in the number of pairs on a chip.

12.4 A conditional prediction

Four things must come first (prediction, conditional): a pair that works in hardware as in the model (gate RG1), the diodes of Section 11.5, pump sources at twice each carrier, and a pump efficiency that holds as the carrier rises.

The rule is that of fixed voltages. Dividing times, capacitances and inductances by α raises the clock, lowers energy per decision and raises the relative noise power, each by α. Shrinking diodes and capacitors by β in area, and raising inductances and resistances by β, lowers energy per decision and raises that noise power by β.

The steps. A pair spends 0.50 pJ per slot at 225 GHz and 0.10 pJ in the 1-THz-class cell. With a third of the diode area that cell would spend 31 fJ at 16 times the 225-GHz design's noise power, where no layout of Section 9 errs without spread. With a thirteenth it would spend 8 fJ at 64 times, where the eight-bit adder and the accumulator first err.

The bound. Without spread and with full shot noise, noise ends the rule between 31 and 8 fJ. A shot-noise factor above 1 would end it earlier, by an amount not run (Section 9.5). Only the step to the 1-THz class was run with all nine spreads (pump phase error 10 degrees).

If these conditions were met, which nothing in this Part shows, the fabric of pairs, not the graphene-plasmon fabric of Parts I to III, could at most start a trajectory of the kind of Moore's law. It would have two steps, a clock 4.78 times faster and about one decade less energy per decision before the pump. Its margins were found without spread and with every parasitic left out. Noise bounds it, and heat does unless pairs are spread out.

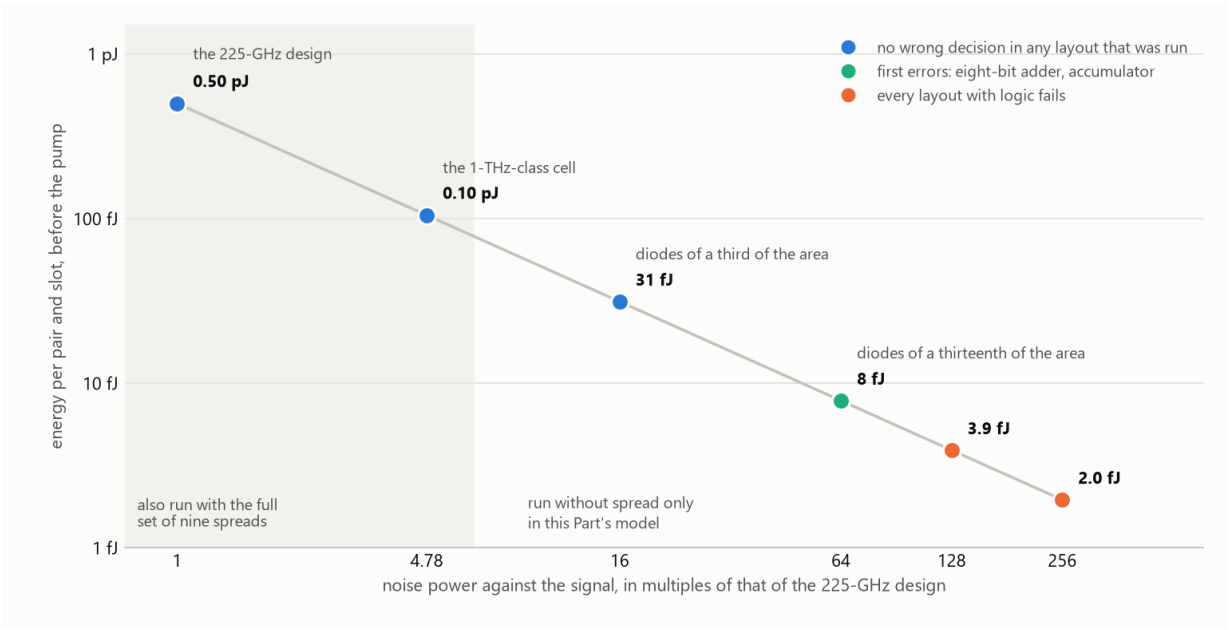


Figure R9. The steps of the scaling rule (prediction, conditional, on in-model runs). Energy per pair and slot, before the pump, against the noise power; the rule keeps their product fixed, and both of its steps leave the model's equations unchanged (this paper's arithmetic). The colour says what the layouts of Table R17 do at that noise power, without spread and with full shot noise. The point at 1 is the operating point of Section 8, and the eight-bit adder was not run at 4.78 times without spread. In the shaded range the four-bit adder was also run with the full set of nine spreads, whose pump phase error is 10 degrees (Section 8.5).

13 Falsifiability

Nothing in this Part has been built. Four experiments, each needing the one before, would show whether the scheme exists. They are stated as gates in the sense of Parts I to III: pre-registered measurements with a pass threshold, not logic gates. Table R25 gives each with what is measured and what the model predicts. The pass thresholds are set by the author before deposit.

Table R25. The four gates. The model targets are in-model results of this Part's circuit model, for the 225-GHz design at 0.94 V with a 25 % pump unless stated. The targets of RG2 to RG4 are read from rows of sixteen and from the carry loops of the serial adder and the accumulator, which are dual-rail: no layout of two pairs alone or of a ring alone was run.

Gate	What is measured	Model target	Pass threshold
RG1	one pair, biased below its own oscillation threshold, with a pump at twice its frequency	silent without the pump; with it an oscillation at half the pump frequency, on two phases half a turn apart, from each of twelve starting phases; on those two phases within about 10 ps after a seed of 28.7 ps ends, at the supply levels below 0.97 V at which it oscillates; for the 160-GHz pair with a 10 % pump at 0.94 V, within 47 ps of the start of a seed of 40 ps	to be set by the author before deposit
RG2	two pairs linked through their inductors and switched on one after the other	with the pump of the second pair stepped by three quarters of a turn and a link of 6 %, the second pair takes the sign of the first; its axis turns by 133 to 136 degrees of carrier phase	to be set by the author before deposit
RG3	one pair with three inputs	the pair takes the majority, also when the vote is two against one	to be set by the author before deposit
RG4	a ring of four pairs, one per clock phase, with one inversion: a reversed link, or two rails crossed as in the layouts that were run	the ring keeps a bit from slot to slot, and a majority gate in the ring sets and clears it	to be set by the author before deposit

RG1 needs no logic and no fabric of pairs. It needs one pair and one pump source. A pair tuned to a 160-GHz carrier with a 320-GHz pump is the one version that a published device might pump. In the model that pair oscillates on two phases from a supply level of 0.94 V with a 10 % pump, and from 0.91 V with 15 % (in-model, one pair alone; Section 2.4). Such a pump takes 0.01 to 0.06 mW for 10 to 15 % (this paper's arithmetic). ROHM's device gives 40 µW at most [5], so it could pump that one pair only if most of its power reached it (external, release and presentation). The input of the pair would have to be derived from the same

source, so that the two stay in step (design). The 160-GHz pair has the diode of the 225-GHz design, a tank of 22.5 fF and 37.7 pH per half and a damping resistor of 9.5 Ω (design). Listing r1_pair of the package reruns it (Appendix RA).

How RG1 can fail. Three outcomes would each fail it. The pair has no supply range in which it is silent without the pump and oscillates with it. Or it oscillates with the pump, but not at half the pump frequency. Or it does so, but its phase against the pump does not fall on two values half a turn apart. This Part names three things that could produce such an outcome and that its model does not settle. They are the in-phase mode (Section 6.5), a low-frequency oscillation of the bias network (Section 14), and a diode curve that differs between peak and valley from the assumed one (Appendix RA).

What RG1 would not show. A passed RG1 shows the effect on which the scheme rests. It shows nothing about links, about majority, about a clock in four phases or about a pump plane. RG2 to RG4 take those in turn, and none of them reaches the pump distribution, the supply network or the spreads of a large machine (Section 14).

If RG1 fails, nothing physical in this Part survives.

14 Status and limitations

Demonstrated (runnable). Nothing physical. The listings of the package rerun the single pair, a row, the four-bit adder, the serial adder and the change of units on a processor. They rebuild the spread budget and the tables from the stored runs, and they print the numbers quoted from them (Appendix RA). That is a check that the released code does what this Part says, not a check of physics.

In-model. Every statement about pairs, rows, adders and layouts with state: levels, phases, working ranges, tolerances, counts of wrong decisions, the spread budget, the sensitivity to stray capacitance, the noise margins, the behaviour at other carriers and with other diodes, and the 1-THz-class cell. All of it is computed in one circuit model with ideal pump, clock, inputs and outputs. The serial adder was also computed by three other codes, rows of sixteen by two and the four-bit adder by one, within the lines listed in Section 11.4 and Appendix RA.

External. The two devices of Section 2 [4, 5], and the diode figures scaled from one of them [4]. The literature on parametrons and on phase logic [18 to 25], on earlier logic of series negative-resistance devices on a clocked supply [39 to 43], and the RTD literature on dividers and on locking [26 to 31]. The shot-noise factor measured at 77 K [32]. The figures of published diodes [13 to 16], and of RTD oscillators and other sources near 1 and 2 THz [6 to 12, 17, 33 to 37]. Appendix RC gives the level at which each was read.

Open. Whether a pair of RTDs pumped at twice its frequency settles on two set phases at all (gate RG1). The pump plane and its source. The electrical clock in four phases. The spreads that a machine of thousands of pairs may have. The diode of the 1-THz class.

Table R26. What is not shown. The second column says what the model assumes, the third what is known.

Part	What the model assumes	What is known
The pair itself	the pair of Section 6	a literature search found no RTD reported to oscillate at half a pump frequency on two set phases; the nearest report is a divider with RTDs and transistors [26] (index abstract)
The pump plane	an ideal pump term of 235 mV in the supply source of every pair, its phase stepping by three quarters of a turn between clock phases	one published array locks 36 oscillators on a chip and radiates the power [4]; delivery to supply nodes, locking to the input reference and four phases are shown nowhere; rows hold with an rms pump phase error from pair to pair of 10 degrees, and the adders are clean at 20 (Sections 7.3 and 8.4); about one pump RTD per logic pair (this paper's arithmetic)
The supply clock	four phases at 14.4 GHz with edges of 14.3 ps; a pair draws 10.5 mA while on	not designed; an eight-bit adder switches about 0.45 A per clock phase (this paper's arithmetic); the four-bit and serial adders and the accumulator are clean, and a row holds, with a timing error of 5 % of the period, 3.5 ps rms (32 runs each); a row fails at 10 %; the eight-bit adder and the adder on two rails were not run with this error alone

Part	What the model assumes	What is known
The supply level at each pair	the same at every pair	the four-bit adder, the serial adder and the accumulator stand an error of 2 % rms, 19 mV (32 runs each, with a 3 % spread of the inductance); at 3 % the four-bit adder has wrong additions in 3 of 32 runs, and the serial adder a wrong decision in 1 run and no wrong sum; at the noise of the 1-THz-class cell these are 5 of 32 runs and 2 wrong sums; the eight-bit adder was not run with this error; one ohm of difference in a supply path is already 10 mV; a difference of peak voltage between the two diodes of a pair was not run
The links	a mutual inductance of 1.58 pH per link, within 10 %; no other coupling	no layout was drawn and no field was computed; stray capacitors of 0.096 fF per link and 0.48 fF at each pair end cost the top of the supply range, the 40 % pump level and the 9 % link strength, and with the full set of spreads (pump phase 10 degrees), at the noise of the 1-THz-class cell, the four-bit adder then fails in 21 of 256 draws against 7 (Section 8.6); a stray inductive coupling between neighbours cost nothing up to 1.2 % in the four-bit adder on one rail and up to 0.6 % on two rails, where 1.2 % gives wrong pairs
The damping resistor	9.3 Ω in each half winding, equal within 10 % from pair to pair	a design choice; not drawn; the adders stand a spread of 10 % rms, and the four-bit adder fails at 15 % (Section 8.4)
All spreads together	nine spreads at once	with the full set, whose pump phase error is 10 degrees, the four-bit adder fails in 5 and in 7 of 256 draws at the two noise levels; at three quarters of it in none and in one of 256; with 32 draws at the noise of the 225-GHz design the accumulator has 4 wrong words of 128, in 2 of 32 draws; two samples of the full set at the noise of the 225-GHz design differ (3 of 32 and 5 of 256 draws, P = 0.048); with the seven spreads at a pump phase error of 20 degrees four of the five layouts each have wrong results in 1 run of 32 at the noise of the 225-GHz design (Sections 8.2, 8.3 and 8.5); a budget for thousands of pairs was not established (Section 8.5)
Inputs	an ideal current of 0.4 mA at the carrier, aligned with the pump	a signal at the carrier locked to half the pump and switched in sign by the data: not designed; a row fails when the input lies 0.875π or 1.0π of pump phase above the aligned value, with a 3 % inductance spread at the noise of the 225-GHz design (32 runs per phase); at 64 times that noise power, without spread, it holds at 12 of 16 input phases (Sections 7.3 and 9.2)
Outputs	the phase of a pair is read against the run without noise	a detector that compares a pair with a reference pair: not designed
Constants	input pairs that always carry 0 or 1	pairs driven by the reference: not designed
Bias stability	a supply source of 2.5 Ω	every RTD oscillator needs a network against low-frequency oscillation; the published array has one at every antenna [4]
The in-phase mode	suppressed by the pump	it grows without a pump between 1.00 and 1.06 V, and with a 5 % pump from 1.01 to 1.06 V; with a 10 % pump it decays, only slowly from 1.02 to 1.05 V (Section 6.5)
The diode	a fitted curve; delay and contact assumed; full shot noise	no measured high-frequency model of the published device was found; a shot-noise factor of up to 6.6 has been measured at 77 K [32]; none was found at room temperature
Diodes of the 1-THz class	the cell of Table R21, and pairs with other diodes	with junctions from 0.52 to 1.25 fF and a contact of 12 Ω the four-bit adder is clean with a 3 % spread, and the serial adder has one wrong sum in one run of 32 on one of the nine pairs (the noise of the 1-THz-class cell); pairs with a junction of 1.7 fF hold rows but fail the four-bit adder in 24 to 32 of 32 runs and the serial adder in 13 to 30, with a 3 % spread; why their gates come up so weak was not found (Section 11.5)
Wires, radiation, substrate	none	nothing was computed
Heat	not modelled	7.2 mW per pair; 1.2 W for the eight-bit adder; in the 1-THz class the same power sits on 1/4.78 to 1/23 of the area (this paper's arithmetic); the cap of 80 °C is neither met nor tested
Larger machines	adders of up to 169 pairs, an accumulator of 84	fan-out above three, long wires, clock and pump distribution across a chip, and yield were not studied
Error rates	counts in at most a few hundred runs	no rate at the noise of either cell is claimed
The 1-THz-class cell	Section 11	no such diode and no such pump source is published; everything the model leaves out must shrink by 4.78 as well; the supply path of a pair must stay below about 4 pH to keep a supply error of 14 mV under edges of 3 ps (this paper's arithmetic)
Codes	one model for most lines	only one pair, rows of sixteen, the serial adder and four supply levels of the four-bit adder were run by other codes; every single tolerance, the full set of spreads, the eight-bit adder, the adder on two rails, the accumulator, rows of 92, the other carriers and the other diodes were run by this Part's model only; at the edges the codes differ, unexplained (Section 11.4)

Part	What the model assumes	What is known
Numerics	a time step of 11.9 fs in single precision	half the time step and double precision were checked on rows and on the serial adder only (Appendix RA); the four-bit and eight-bit adders, the adder on two rails, the accumulator and the spread budget were not repeated; the alternation in sign, from step to step, of the voltage across the stiff 1-Ω stub resistor was not tested for its effect on decisions (Appendix RA.2)

Runs that were not made.

- The spread budget on a layout larger than 53 pairs, and with more draws below three quarters of the full set.
- The full set of nine spreads on the eight-bit adder at either noise level, on the accumulator at the noise of the 1-THz-class cell, and on any pair with another diode.
- The full set of spreads together with a noise above 4.78 times, and a shot-noise factor above 1 as such.
- A difference of peak voltage between the two diodes of a pair, and a diode with the lower ratio of peak to valley of the fastest published diodes.
- Adders on the variants of Section 10.1, and single tolerances at any carrier other than 225 GHz and 1.075 THz.
- Supply levels between those listed. Rows were scanned in steps of 15 mV. The four-bit and serial adders were run at eight levels from 0.880 to 1.015 V, the eight-bit adder and the accumulator at 0.910, 0.940 and 0.970 V only.
- The four-bit adder on the pair with 1.25 fF and 24 Ω at a supply level inside the range of its row (Section 11.5).
- The in-phase mode of a single pair with a pump above 30 % (Section 6.5).
- A supply path and a pump feed with a finite impedance.
- Circuits for inputs, outputs and constants.
- The reported batches in double precision. Double precision was run for the reference runs of two layouts and for the serial adder at the top of the supply range (Appendix RA).

15 Conclusion

What computes. In a circuit model, a pair of RTDs on a metal inductor, biased just below its own threshold and pumped at twice its carrier, is silent without the pump and settles on one of two phases with it. Rows of such pairs carry bits and restore them. Adders of 53 and 169 pairs, a serial adder and an accumulator give no wrong result at the operating point in 32 runs per line, with noise and with an inductance spread of up to 5 %. They do so at a 225-GHz carrier and, in the 1-THz-class cell, at its own noise (in-model, in one code except where Sections 8.7 and 11.4 name other codes; counts, not rates; full shot noise assumed). The 1-THz-class specification is validated in the model only, and there within the lines run (Section 11.4).

What binds. These are in-model results, with this paper’s arithmetic and external figures where sources are cited.

- The supply level from pair to pair: with a 3 % inductance spread, the four-bit adder stands an error of 2 % rms and fails at 3 %, at the noise of either cell (32 runs per value; counts).
- All nine spreads together, with a pump phase error of 10 degrees, with which the four-bit adder fails in 5 and in 7 of 256 draws at the two noise levels (in one code; counts).
- Stray capacitance between pairs (Section 8.6).
- In the 1-THz class, the diode. The specified cell asks 3.3 to 5 times the current per capacitance of the fastest published diode. Pairs with junctions up to 1.25 fF and a contact of 12 Ω ask 1.4 to 2.1 times. On them, at the noise of that cell with a 3 % inductance spread and 32 runs per line, the four-bit adder was clean and the serial adder had one wrong sum in one run on one of the nine pairs. The contact of the cell is 1.5 to 2.5 Ω µm² at published current densities and about 0.5 Ω µm² at the published capacitance per area, against 2 to 3 reported at best [13]. With the present junction the contact would have to be about 0.6 Ω µm² (Section 11.5).
- The pump: a source about 170 to 250 times stronger than the 0.6 µW at 2.06 THz [34] and the 0.4 µW at 1.92 THz found on a chip ([8], abstract; the power from the thesis [13], secondary, and not stated as continuous).
- The power: half a picojoule per pair and slot at 225 GHz, before the pump.

What decides. One experiment: one pair, biased below its threshold and pumped at twice its frequency. A literature search found no RTD reported to do what the model's pair does (external; a literature search). If the pair does not, nothing physical in this Part survives.

None of the in-model statements is yet a measurement.

Appendix RA The model and the package

Section 5.5 gives the equations of one half of a pair. This appendix adds what a reader needs to rebuild the model, then the numerical checks, the package and the other codes. The file MODEL.md of the package writes all of it out from the code, with every constant.

RA.1 The rest of the model

The diode law. At a diode voltage u, the static current of the full published device, in mA, is

$$J(u) = 0.9333\,[\,A\,(sp(a_+) - sp(a_-))\,(\pi/2 + \operatorname{atan}((C - n_1 x)/D)) + H\,(\exp(n_2 x/V_T) - 1) + 2.218 \tanh(x/0.05)\,] \qquad \text{(R8)}$$

$$a_\pm = (B - C \pm n_1 x)/V_T, \quad x = u/1.667, \quad sp(z) = \ln(1 + e^z) \qquad \text{(R9)}$$

with A = 3.541, B = 0.1002, C = 0.1480, D = 0.02606, n_1 = 0.2882, n_2 = 0.1843, H = 0.007984 and V_T = 0.025852 V. It has a peak of 25.39 mA at 0.750 V and a valley of 11.40 mA at 1.300 V. A, H and the factor 2.218 are in mA, B, C, D, x and V_T in volts, and n_1 and n_2 are numbers. V_T is the thermal voltage at 300 K: the exponent of the law is kept at 300 K, while the noise is computed at 353 K. The code of this study names the physics-based law of [38] as the source of this form (not read). The constants A to H come from a fit to another diode, made in an earlier trial of this project. The three factors 0.9333, 1.667 and 2.218 scale the current, stretch the voltage axis and add valley current, so that the peak, the valley and the voltage between them are those that the source fits [4]. The shape between peak and valley is an assumption.

The clock window. With E the edge time and g(y) = 0.5 − 0.5 cos(π clip(y/E + 0.5, 0, 1)), a pair at clock depth d has the window

$$w(t) = g(\tau) - g(\tau - \delta T) + g(\tau - T), \quad \tau = T\,\mathrm{frac}(t/T - d/4) \qquad \text{(R10)}$$

with δ = 0.75. The supply rises centred on the start of the pair's period and falls centred on δT. The pump of (R7) is multiplied by the same window.

The start ramp. During a first time t_r of every run the supply, with its pump, is also multiplied by a linear ramp, so that (R7) reads $v_{clk}(t) = V \min(1, t/t_r)\, w(t)\, [1 + p \cos(4\pi f t + \theta_d)]$. The time t_r is 14.3 ps in the 225-GHz design and 3 ps in the 1-THz-class cell.

The drive. An input pair receives a current of ±0.4 mA cos(2πft) into its two ends, in antiphase, with the sign of its bit. The drive is on from a quarter period before the pair's slot starts until the pair switches off, and switches without a ramp. Every run starts from zero, with no kick: a run without noise starts from the drive alone.

The stub. The lead at which a pair is driven and read is a lossless line of four sections behind 1 Ω, 0.637 fF and 6.37 pH in all for the 225-GHz design. It is short, with a one-way delay of 0.06 ps.

The links. A link is a mutual inductance between the antiphase modes of two pairs, by (R5). Each winding of one pair shares half of M with each winding of the other, with the signs of the antiphase mode: like windings share +M/2 and unlike windings −M/2. The inductance matrix of all windings of a layout is inverted once. Its blocks inside a pair enter the implicit step, and the blocks between pairs enter as a source taken at mid-step.

Noise. Every resistor has a white voltage source of its thermal noise at 353 K. The shot noise is a random charge step of variance $q|i_x|\Delta t$ on each junction in each time step Δt, with q the elementary charge. That is full shot noise, an assumption. A common factor multiplies the power of all sources: 0.209 for the 225-GHz design and 1 for the 1-THz-class cell at its own noise.

Spreads. Every spread is a normal draw, one per run and pair unless it belongs to a link or a clock phase, and zero in the reference run. The draws are not cut off. An inductance spread changes both halves of a pair alike and the links with them. A supply level error scales the pump with it. A clock timing error moves both edges of

a pair and not its pump. A pump phase error is given in degrees of the pump wave, so that 10 degrees of it are 5 degrees of carrier phase.

RA.2 Integration and its checks

The lumped equations are stepped with the trapezoidal rule and the stub with a staggered scheme, at a time step of 11.9 fs for the 225-GHz design. The reported batches ran on a graphics processor, with the state in single precision. The listings of the package run the same code in double precision on a processor. All checks below are in-model, in this Part's code.

- **Half the time step,** on a row of sixteen at the operating point, changes the phase of a pair by at most 0.19 degrees. It changes its level by at most 0.1 % at the decision and 0.2 % at the end of the on-time (the reference run and 32 runs with a 3 % spread of the inductance, without noise). With noise the row has no wrong decision at either step, and the same phase error of 3.8 degrees at pair 14.
- **At the ends of the supply range, without noise, the changes are larger and change no decision:** at 0.880 V up to 2.4 % in level, and at 1.015 V up to 1.0 % in level and 1.04 degrees in phase, read at the decision.
- **Single against double precision.** Runs without noise or spread in double precision agree with the stored single-precision runs within 0.01 mV in level and 0.01 degree in phase, for every pair and every counted slot of the row of sixteen and of the serial adder at the operating point. In the first slot of the serial adder, which no count uses, levels differ by up to 0.08 mV. The mean supply power of the row, which no table uses, differs by 0.1 % between the two, and the cause was not found.
- **A stub of eight sections instead of four,** with half the time step, gives the same figures as half the time step alone within 0.01 degree, on the row of sixteen. It was not run on the serial adder.
- **The serial adder at half the time step** differs by at most 0.20 degrees and 0.1 % at the operating point, read at the decision (the reference run and 16 runs with a 3 % spread, without noise). With noise it has no wrong decision at either step.
- **The top of the supply range in double precision.** The serial adder was run at 0.985, 1.000 and 1.015 V in double precision on a processor, at the standard and at half the time step, with noise and a 3 % spread. None of the six lines has a wrong decision among 19,840 in 32 runs. The reference runs at the two steps differ by at most 0.39 degrees and 0.4 % in the phase and level read at the decision. In those read at the end of the on-time they differ by at most 1.4 degrees and 1.3 %, which is 2.5 mV at 1.015 V.

MODEL.md of the package, section 8, states these comparisons twice. First it gives the largest change in millivolts over three readings of the level and over a whole batch, which is at most 1.3 %. Then it gives the change read at the decision alone, which is the reading above: at most 2.4 % at 0.880 V, the supply level at which the levels are lowest.

One element of the integration is stiff. The 1-Ω resistor between a pad and its stub has a time constant far below the time step, and the trapezoidal rule then lets the small voltage across it alternate in sign from step to step, by a factor of −0.974 per step. Halving the time step moves that factor only to about −0.95 and does not remove the alternation. Its effect on decisions was not tested.

RA.3 The package

The model, the listings and the stored runs form the package `fable-model-parametron`. It is pure Python and needs only numpy. Seven listings rerun or rebuild the central results on a processor, each in a few minutes or less, and print every number they compute. The output of each on the computer of this study is stored beside it.

Table R27. The listings of the package (demonstrated (runnable): each reruns part of the model or rebuilds results from the stored runs, and prints the values quoted here; none is a check of physics). Every entry is at 0.94 V with a 25 % pump and links of 6 %, without the stray capacitors and at the noise of the 225-GHz design, unless stated.

Listing	What it reruns	What it prints
r1_pair	one pair on a constant supply	the range in which the pair oscillates by itself, 0.97 to 1.14 V; two phases with a 25 % pump at 0.94 V, six of twelve starts on each; every entry of Table R4; with the option cell=c160, the same for the 160-GHz pair of Sections 2.4 and 13

Listing	What it reruns	What it prints
r2_row	a row of sixteen at the operating point	16 of 16 pairs right; 230 mV per half when the next pair decides; a turn of 133 to 136 degrees of carrier phase per link, 135 degrees as the median along the row; no wrong decision of 3,360 in 32 runs with a 3 % spread
r3_adder	the four-bit adder	53 of 53 pairs right, lowest level 200.5 mV; no wrong addition of 248 in 8 runs with a 3 % spread
r4_serial_adder	the serial adder without and with the stray capacitors of Section 8.6	weakest levels, read in the common way of the comparison of codes: 205.1 and 266.5 mV at 0.94 and 1.015 V without them, 198.0 and 196.9 mV with them; at 0.94 V without them, no wrong sum in 16 runs with noise and a 3 % spread
r5_units	the 225-GHz design and the 1-THz-class cell as one calculation	the two sets of units give the same traces to 10^{-13} of the signal
r6_spread_budget	the spread budget from the stored runs; four draws of the full set run and judged	the lines of Table R15 with their intervals; how a draw of the nine spreads is made
r7_tables	the tables of results, rebuilt from the stored runs	eight tables, every line with its batch

The listings draw their noise from another generator than the batches did, so their counts with noise are checked as counts and not bit for bit. A further script compares the packaged code with the code as it ran, on stored arrays, bit for bit.

Stored runs. For every batch of this Part the package stores the settings and the result index, and for the 42 batches that have one, every analysis file, with a manifest of sizes and checksums. Five check batches, those of time step, stub and precision, have no analysis file. The arrays of levels and phases, files of up to 55 MB each, and the large summary files are not in the package. A script rebuilt all 55 analysis and summary files of the 42 batches from the arrays and found every one of them bitwise equal. The package also holds the specifications from which the other codes were written, and those three codes with their reports.

Table R28. Where each exhibit of this Part comes from. Batches are named as in the package.

Exhibit	Batches or source
Table R3, its in-model lines	listing r1_pair; g29
Table R4	single-pair runs; listing r1_pair
Figures R3 and R4, Section 6.4	single-pair session runs, not in the package
The 160-GHz pair of Sections 2.4 and 13	single-pair runs; listing r1_pair with the option cell=c160
Table R5	single-pair runs with an in-phase start; rows of eight and the serial adder read in phase; session runs, not stored as batches
Table R6, Figure R5	g28a
Table R7	g28f
Table R8	g28a, g34a, g54e
Table R10	g28b, g37a
Table R11	g28e, g37b, g41x, g41, g28g
Table R12	g28c, g31, g37d
Table R13	g28d, g34d, g43
Table R14	g28b, g28c, g28g, g34b, g34c, g40
Table R15, Figure R6	g52, g53; the lines of 32 draws in g34b, g34c, g40 and g42
Table R16	listing r4_serial_adder; g28c and g31 for the runs without the strays; older batches with the capacitors, not in the package, for the runs with them; g52 for the line with the full set in the text
Table R17, Figure R9	g28a, g28b, g28c, g28d, g31, g34a, g36a, g41x, g54a to g54e; the third code's run at raised noise from its log
Table R18	g33
Table R19, Figure R7	g32
Table R20	g35a; the serial adder in g35b and g37d
Table R22	g40, g42, g48, g49; the eight-bit adder and the accumulator in g41x, g41, g43, g50 and g51
Table R23, Table R29	the logs of the other codes; listing r4_serial_adder for this Part's model
Table R24, Figure R8	g39, g46; the adders on those pairs in g42, g44 and g47

RA.4 The other codes

Three further codes of the circuit were written by agents that did not see this Part's code.

- **The second code** was written in four stages by four modellers, from a specification of the 225-GHz design and its two addenda. The stages were the pair and a row; the serial adder; rows with the pump step of three quarters of a turn; and the serial adder with that step. The four shared one file for the cell, so their work is one code and not four. It ran at the noise of the 225-GHz design and, through the change of units, at 4.78 and at 16 times that noise.
- **The third and the fourth code** were each written by one modeller from one stand-alone specification of the 1-THz-class cell, in that cell's own units, with the noise taken from the thermal and shot-noise powers directly. Neither modeller saw anything else of the study. Each chose a second-order implicit integrator of its own and checked its time step by halving, on runs without noise at 0.94 V only.

The stand-alone specification of the 1-THz-class cell differs from this Part's model in small points. It has one node with a capacitor where the model has a stub of four sections. It repeats the bit pattern of a row where the model runs it once. It gives 5.5047 pH for the antiphase inductance where the model has 5.5037 pH. It does not mention the start ramp of the model's supply. And it asks for a reading window of one to a few carrier periods, a little after a quarter period into the slot, and leaves its exact place to the modeller.

What each code ran. The second code ran one pair, rows of sixteen over supply level and pump level, and the serial adder over supply level, pump level and link strength, at both noise levels. The third ran one pair, rows of sixteen and the serial adder, with 16 runs per line, and the serial adder once at raised noise (Section 9.2). The fourth ran one pair, the serial adder at three supply levels and the four-bit adder at four. No other code ran the eight-bit adder, the adder on two rails, the accumulator, any single tolerance, the full set of spreads or its fractions, rows of 92, other carriers or other diodes.

One pair. In all three codes the pair oscillates by itself from 0.97 to 1.14 V, as in this Part's model. With a 25 % pump at 0.94 V the third and the fourth find the oscillation at half the pump frequency on two phases half a turn apart, with six of twelve starts on each.

Table R29. Weakest level of any pair of the serial adder without noise or spread, in mV (in-model, three codes). The first two codes are read in one common way, the third with its own window of the same length.

Supply level	This Part's model	Second code	Third code
0.940 V	205	201	202
0.985 V	253	251	251
1.000 V	262	261	261
1.015 V	267	264	263

The weakest levels of the three codes agree within 2.1 %. The largest difference is at 0.94 V, between this Part's model and the second code.

With noise and spread. At the noise of the 225-GHz design, with a 3 % spread and 32 runs, the serial adder of the second code is clean wherever this Part's model is, with two differences. It has 14 wrong sums against 18 at 0.880 V, and one wrong sum in one run at a 40 % pump where this Part's model has none. Its lines on link strength have 16 runs. Section 11.4 gives the comparison of all four codes at the noise of the 1-THz-class cell, and Section 7.4 that of the rows.

At the edges of the working ranges the codes differ in their counts (Section 11.4), and in two lines on rows in the verdict itself (Sections 7.4 and 11.4). Those differences were not explained.

Appendix RB Corrections and checks

The study behind this Part was wrong several times, and each error was found by a run, a second code or a reader. This appendix lists them, because a reader who knows how a result was reached can judge it better.

RB.1 The capacitors

The largest error concerns every batch of the first complete suite. The model had been inherited from an earlier trial in which pairs were linked across small gaps. When the links were moved to the inductors, the gap capacitance was reduced to 0.096 fF per link and was not removed. Each pair end was also padded so that it carried 0.48 fF in all in the adders and 0.57 fF in the accumulator, its link capacitors included. The study's report described the links as mutual inductances only, and the specification that the second code was written from did so too.

The second code then disagreed at the top of the supply range: at 1.015 V the serial adder erred in 19 of 32 runs in this Part's model and in none in the second code. Two investigators, one by measurement and one by reading the code against the specification, each found the capacitors and closed the difference in both directions: this Part's model without them reproduces the second code, and the second code with them reproduces the errors. Every batch of the adopted design was then run again without the capacitors. This Part reports those runs, and runs with the capacitors only where it says so (Section 8.6).

With the capacitors the reported ranges had been too narrow at the top of the supply range, at a 40 % pump and at links of 9 %, and slightly too wide at the lowest supply level. The single tolerances were the same within one step. With the full set of spreads (pump phase error 10 degrees), at the noise of the 1-THz-class cell, the four-bit adder with the capacitors fails about three times as often: in 21 of 256 draws against 7 (Section 8.6). The error became a result: the design is sensitive to stray capacitance between pairs.

RB.2 Earlier corrections

Table R30. Where the study was wrong during the work, and what corrected it.

What was wrong	What corrected it
The first operating point lay in the middle of the range in which the pair oscillates by itself; rows then failed a 2 % spread of the inductance	a scan of the lower edge of that range; the single-pair runs showed why (Section 6)
Rare failures of rows were blamed on the inductance spread	regenerating the random draws showed that every failure began at the driven pair: the input lay about 70 degrees of carrier phase off the pump's axis
The serial adder's failures were blamed on its clock	with the input aligned it is clean at the original on-time
Gates were judged at the end of their on-time, and 30 of 169 pairs seemed wrong	a gate is pulled late in its on-time by the pairs it feeds; judged when the next pairs decide, all are right
The pump step of three quarters of a turn was ruled out because it inverts a bit round a loop	one inversion in the loop removes it: a reversed link, or a crossing of the two rails in the dual-rail layouts that were run
A second code was compared with the wrong map, and an agreement was reported that was partly an artefact	checkers
Failures at 640 and 900 GHz were taken for limits of the diode	they were results of the first pump step and the first input phase; reruns moved them
The spread that matters most, the supply level from pair to pair, had been left out	a theory reader had named it; checkers asked for the run
Published diodes were read too kindly: the current density of one diode was divided by the capacitance of another	two rounds of checkers; the references were then read at their sources (Appendix RC)
The loss that the contact adds was measured as the contact resistance times the capacitance, on a checker's proposal that was not checked	the next round of checkers derived the right measure: the contact resistance times the square of the capacitance (Section 11.5)
The outlook counted on noise margins measured without spread and left out the power density	checkers
The runs of the 225-GHz design were called runs of the 1-THz-class cell at its own noise; they are that cell at a fifth of its noise	a reader who had seen nothing before; the missing runs were made
Four rebuilds of the design were called four independent codes; they shared one cell model	reading the code; two further codes were then written from a stand-alone specification
Counts of 32 draws were used to judge a failing share of a few per cent	batches of 256 draws (Section 8.5)
A figure of 15 µW at 1.55 THz was quoted as contested; it is a citation slip in a thesis	the check of the references at their sources

RB.3 The checks

The study's report went through three rounds of four checkers each and two last readers. A ledger of its claims was built against its tables. The references were checked at their primary sources by three readers. The model's equations were written out from the code by one reader and checked against the code by another. The note that corrected the report after the capacitors were found was checked by a numbers reader and by a reader of its framing. The package was built by two agents, tested by two others who ran it as strangers, and fixed by a fifth. This manuscript was drafted section by section by the session's main thread. Each part was then checked against its sources by an agent, eight in all, and the main thread applied their findings. Three further readers then read the whole: one for numbers, one for claims and one as a referee. Two readers went to the sources of the two earlier logic families of series negative-resistance devices that the referee named (Section 3). The main thread applied the findings of all five, and two last checkers went through those changes. Their findings were

applied too, and one more checker compared that last set of changes with their reports. What that checker found was applied as well, and no agent checked those last few changes again. All of these were AI agents working at the author's direction (see the disclaimer). No human expert has reviewed the model or this text.

Appendix RC Sources and how each was read

Five readers of the literature and three checkers of the references went to the primary sources where they could be had. Seventeen sources were not read in full, and three of them were not read at all. Table R31 gives, per reference, what this Part takes from it and at what level it was read. "Full text" means the paper, patent or page itself was read; "abstract" means the abstract or an index record; "secondary" means the figure is known through another source that was read.

Table R31. Sources and reading levels.

Reference	What this Part takes from it	Read
[4]	Canon's array: every figure of Section 2.2; the diode figures behind Table R3; the efficiency used in Sections 2.4 and 12	full text, open access, by two readers
[5]	ROHM's device: every figure of Section 2.3; the 40 µW used in Sections 2.4 and 13	release and presentation, in full
[6]	the highest RTD fundamental, 1.98 THz	not read; the frequency through [7] and [14]
[7]	1.98 and 1.92 THz as record frequencies; no power for either	full text
[8]	1.92 THz; its 0.4 µW through [13]	abstract
[9] to [12]	RTD powers from 0.65 to 1 THz	abstracts; for [10] also the first author's thesis, in part
[13]	current densities, peak-to-valley ratios and powers of the fastest RTDs; contacts	full text; secondary for other groups' devices
[14]	capacitance, delay and current density of the 1.98-THz diode; the definition of the delay	its table and the passages on delay, at the publisher's open page; full text by one reader
[15]	fitted delays of two diodes; a measured contact	full text, an archive copy
[16]	a capacitance of 3.3 fF/µm², assumed there and stated as verified by test measurements, at 12 mA/µm², for oscillators at 0.4 to 0.8 THz (Section 11.5)	full text; a preprint
[17]	2.2 µW at 1.74 THz	accepted manuscript, in full
[18]	the parametron	abstract
[19]	parametron machines	a secondary page
[20]	majority organs and supplies in three phases	patent text, machine-read
[21]	microwave phase logic of 1961	abstract
[22]	the tunnel-diode pair of Section 3	patent scan, in full; parts of four columns are hidden
[23], [24]	phase logic with self-sustaining oscillators	full text
[25]	the adiabatic quantum flux parametron, which Part I names without citing a paper on it	not read; the first author's thesis was read
[26]	a divider by two with RTDs and transistors at 88 GHz	index abstract
[27]	the divider's RTD circuit as a driven oscillator	full text
[28]	an RTD oscillator at about 550 GHz locked by a signal at half its frequency, the opposite case to the pair	full text
[29], [30]	a ROHM prototype at 322 GHz with about 8 µW and its linewidth; ROHM-made devices locked to a signal at their own frequency	full text
[31]	an RTD locked in antiphase to an injected pulse, the locked signal building up in about 50 ps	full text
[32]	a shot-noise factor of up to 6.6 at 77 K	full text
[33]	the wall-plug efficiency of laser sources by difference-frequency generation in continuous operation; its figures are at 3.4 to 3.5 THz	full text
[34]	0.6 µW at 2.06 THz	its full-text page, through a text tool; one figure not inspected by eye
[35]	a multiplier chain, not on a chip: 60 µW at 1.95 THz, nothing at 2.15 THz	full text
[36]	80 µW at 1 THz from a silicon chip	accepted manuscript, in full
[37]	multiplier chains at 1.0 and 1.6 THz	abstract
[38]	the form of the diode law of Appendix RA	not read; the code of this study names it as the source of the form
[39]	the tunnel-diode twin: a series pair, the bit as the polarity at its mid-point, majority, three supply phases, a clock of 30 megacycles per second	abstract, through an index

Reference	What this Part takes from it	Read
[40]	the MOBILE: two negative-resistance devices in series on an oscillating bias; fan-out	abstract
[41]	threshold gates of three weighted inputs with the MOBILE	abstract
[42]	a MOBILE of RTDs and transistors at up to 35 Gb/s	abstract
[43]	a title that names 100-GHz operation of a MOBILE; the gate is edge-triggered and latching	index record and first paragraph

Sources that nobody of this study read in full: [6], [8], [9], [10], [11], [12], [18], [21], [25], [26], [37], [38] and [39] to [43]. No figure is taken from them beyond what the table states.

Two statements of the earlier Parts are touched by these readings, and neither is corrected here. Part III quotes 15 µW at 1.002 THz and 73 µW at 0.863 THz as the best single RTD oscillators near 1 THz (Part III, Section 8.1(e); external there). The source of the second claims the highest power for one simple antenna type only, and the 15 µW at 1.002 THz is not in its abstract [12] (external, abstract). Other reports near 1 THz give 21 µW from separate single oscillators [11], more than the 15 µW and less than the 73 µW. They also give about 0.24 mW at about 925 GHz from two coupled RTDs [10], in a group that measures with a pulsed bias at 50 % duty (external, abstracts; for [10] also the first author's thesis, read in part). Part I quotes RTD oscillation "to 1.92 THz" (Part I, Section 2, citing its reference [29]). That citation is right, and a later device reached 1.98 THz (external, through [7] and [14]; [6] itself was not read). Whether either needs an entry in the project's errata is for the maintainer.

Appendix RD Symbols

Table R32. Symbols.

Symbol	Meaning
V	supply level of a pair while it is on
p	pump level: the amplitude of the pump voltage as a fraction of the supply level
f	carrier frequency; the pump is at 2f
T	clock period; one slot
d	clock depth of a pair: its clock phase, counted in quarter periods
θ_d	pump phase of the pairs at depth d
w(t)	clock window: 1 while the pair is on, 0 while it is off, with edges of finite length
δ, E	on-time of a pair as a fraction of T, 0.75; edge time of the clock window
g, τ	edge function of the clock window in (R10); time within the pair's own period there
v_{clk}	voltage of the supply source of a pair: clock, pump and start ramp
v_b, v_p, v_j	voltages of the supply node and of the pad, and the voltage across the junction
i_L, i_x, i_s	winding current; conduction current of the diode; current from the stub
h	index of the two halves of a pair
C_p, C_d, C_b	tank capacitor; junction capacitance; capacitance of the supply node
ρ, R_b, R_L	contact resistance of a diode; resistance of the supply source; damping resistor of a half winding
L, L_h, k	inductance matrix of the windings; inductance of one half winding; coupling of the two halves of one inductor
M, L_a, L_b, s	mutual inductance of a link; antiphase inductances of the two linked pairs; sign of the link, +1 for one that copies and −1 for one that inverts
J(u), τ_d	static curve of the published device at a diode voltage u; diode delay
x, a_+, a_-, sp	scaled diode voltage, the two arguments and the function of the diode law (R8) and (R9)
A, B, C, D, H, n_1, n_2, V_T	constants of the diode law; C and D there are not capacitances
q, Δt	elementary charge; time step
K	the factor 1.075/0.225 = 4.78 between the 225-GHz design and the 1-THz-class cell
α, β	factors of the scaling rule of Section 12.4, in time and in diode area
P	probability of a two-sided exact test

The letters that name the pairs of an adder stage (A, B, C, G, K, M and S in Section 5.4) are names of pairs, not quantities.

Data and code availability

The model, its listings and the stored runs are released with this Part as `fable-model-parametron/` in the repository of Parts I to III (https://github.com/ryoji-info/FableComputer), beside the released chains of those

Parts, of which it imports nothing. Most in-model numbers of this Part come from the batches named in Table R28. Their settings, result indexes and analysis files are stored in the package; their arrays are not. The scripts beside them rebuild the tables from which this Part quotes. The single-pair table, and that of the 160-GHz pair, are rerun by listing r1_pair. The finer scan of Figure R3, the traces of Figure R4 and the scan of Section 6.4, the in-phase runs and the noisy runs of the serial adder with the stray capacitors come from session runs that the package does not hold, and Table R28 marks them. The numbers of the other codes come from their logs and reports, which the package holds, with the specifications from which those codes were written.

Five listings rerun the single pair, a row, the four-bit adder, the serial adder and the change of units on a processor (Python 3 and numpy). Two more rebuild the spread budget and the tables from the stored runs, and the first of them also runs four draws of the full set. Each prints the numbers quoted from it, with its reference output beside it. The reported batches ran on one graphics processor with the state in single precision. The listings do not rerun them. A settings file reruns any of them, and on a processor the noise then comes from another generator, so that counts with noise compare as counts and not run for run.

Values from Parts I to III and from external sources carry their citations, and Appendix RC gives the level at which each source was read. The arithmetic of this Part is shown where it appears. The revision history is kept in papers/REVISION-HISTORY.md.

References

The references are grouped by subject: the series [1 to 3]; RTD sources and diodes [4 to 17]; phase logic, parametrons and locking [18 to 32]; sources near 1 and 2 THz [33 to 37]; the form of the diode law [38]; earlier logic of series negative-resistance devices on a clocked supply [39 to 43].

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